W25M121AV

Featuring

SERIAL MCP FLASH MEMORY

With Multi I/O SPI & Concurrent Operations

3V 128M-bit Serial NOR Flash Memory
&
3V 1G-bit Serial NAND Flash Memory

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Preliminary – Revision A

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1. GENERAL DESCRIPTIONS

The W25M121AV (128M-bit Serial NOR + 1G-bit Serial NAND) Serial MCP (Multi Chip Package) Flash memory is based on the popular W25Q/W25N ***SpiFlash***® series by stacking W25Q128JV and W25N01GV into a standard 8-pin package. It offers flexible memory density and reliability combination for the low pin-count package, as well as Concurrent Operations in Serial Flash memory for the first time. The W25M ***SpiStack***® series is ideal for small form factor system designs, and applications that demand high Program/Erase data throughput.

The ***SpiStack***® product series introduces a new "Software Die Select (C2h)" instruction, and a factory assigned "Die ID#" for each stacked die. Each W25Q128JV and W25N01GV die can be accessed independently even though the interface is shared. The ***SpiStack***® feature only allows a single die to be Active and have control of the SPI interface at any given time to avoid bus contention.

The W25M121AV maintains all the ***SpiFlash***® features and functions, with the support for standard SPI (Serial Peripheral Interface), Dual I/O SPI, Quad I/O SPI through the shared SPI interface: Serial Clock, Chip Select, Serial Data I/O_0 (DI), I/O_1 (DO), I/O_2, and I/O_3.

The W25Q128JV array is organized into 65,536 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time. Pages can be erased in groups of 16 (4KB sector erase), groups of 128 (32KB block erase), groups of 256 (64KB block erase) or the entire chip (chip erase). The W25Q128JV has 4,096 erasable sectors and 256 erasable blocks respectively. The small 4KB sectors allow for greater flexibility in applications that require data and parameter storage.

The W25N01GV 1G-bit memory array is organized into 65,536 programmable pages of 2,048-bytes each. The entire page can be programmed at one time using the data from the 2,048-Byte internal buffer. Pages can be erased in groups of 64 (128KB block erase). The W25N01GV has 1,024 erasable blocks.

W25M121AV consists of:

- **W25Q128JV**
  - 3V 128M-bit / 16M-byte NOR Flash Memory
- **W25N01GV**
  - 3V 1G-bit / 128M-byte Serial SLC NAND Flash Memory
- **Space Efficient Packaging**
  - 8-PAD WSON – Dimension 8x6x0.8-mm, pad pitch 1.27-mm
  - Contact Winbond for other options

2. FEATURES

W25Q128JV Features

- **New Family of SpiFlash Memories**
  - W25Q128JV: 128M-bit / 16M-byte
  - Standard SPI: CLK, /CS, DI, DO
  - Dual SPI: CLK, /CS, IO_0, IO_1
  - Quad SPI: CLK, /CS, IO_0, IO_1, IO_2, IO_3
  - Software Reset
- **Highest Performance Serial Flash**
  - 133MHz Single, Dual/Quad SPI clocks
  - 266/532MHz equivalent Dual/Quad SPI
  - 66MB/S continuous data transfer rate
  - Min. 100K Program-Erase cycles per sector
  - More than 20-year data retention
- **Efficient "Continuous Read"**
  - Continuous Read with 8/16/32/64-Byte Wrap
  - As few as 8 clocks to address memory
  - Allows true XIP (execute in place) operation
  - Outperforms X16 Parallel Flash
- **Low Power, Wide Temperature Range**
  - Single 2.7V to 3.6V supply
  - -40°C to +85°C operating range
  - <1µA Power-down (typ.)
- **Flexible Architecture with 4KB sectors**
  - Uniform Sector/Block Erase (4K/32K/64K-Byte)
  - Program 1 to 256 byte per programmable page
  - Erase/Program Suspend & Resume
- **Advanced Security Features**
  - Software Write-Protect
  - Power Supply Lock-Down and OTP protection
  - Top/Bottom, Complement array protection
  - Individual Block/Sector array protection
  - 64-Bit Unique ID for each device
  - Discoverable Parameters (SFDP) Register
  - 3X256-Byte Security Registers with OTP locks
  - Volatile & Non-volatile Status Register Bit

W25N01GV Features

- **New W25N Family of SpiFlash Memories**
  - W25N01GV: 1G-bit / 128M-byte
  - Standard SPI: CLK, /CS, DI, DO, /WP, /Hold
  - Dual SPI: CLK, /CS, IO_0, IO_1, /WP, /Hold
  - Quad SPI: CLK, /CS, IO_0, IO_1, IO_2, IO_3
  - Compatible SPI serial flash commands
- **Highest Performance Serial NAND Flash**
  - 104MHz Standard/Dual/Quad SPI clocks
  - 208/416MHz equivalent Dual/Quad SPI
  - 40MB/S continuous data transfer rate
  - Fast Program/Erase performance
  - More than 100,000 erase/program cycles
  - More than 10-year data retention
- **Efficient "Continuous Read Mode"(1)**
  - Alternative method to the Buffer Read Mode
  - No need to issue "Page Data Read" between Read commands
  - Allows direct read access to the entire array
- **Low Power, Wide Temperature Range**
  - Single 2.7V to 3.6V supply
  - 25mA active, 10µA standby current
  - -40°C to +85°C operating range
- **Flexible Architecture with 128KB blocks**
  - Uniform 128K-Byte Block Erase
  - Flexible page data load methods
- **Advanced Features**
  - On chip 1-Bit ECC for memory array
  - ECC status bits indicate ECC results bad block management and LUT(2) access
  - Software and Hardware Write-Protect
  - Power Supply Lock-Down and OTP protection
  - 2KB Unique ID and 2KB parameter pages
  - Ten 2KB OTP pages(3)

Notes:

1. Only the Read command structures are different between the "Continuous Read Mode (BUF=0)" and the "Buffer Read Mode (BUF=1)", all other commands are identical.
   W25N01GVxxIT: Default BUF=0 after power up
2. LUT stands for Look-Up Table.
3. OTP pages can only be programmed.

3. PACKAGE TYPES AND PIN CONFIGURATIONS

W25M121AV is offered in an 8-pad WSON 8x6-mm (package code E) package as shown in Figure 1. Package diagrams and dimensions are illustrated at the end of this datasheet.

3.1 Pad Configuration WSON 8x6-mm

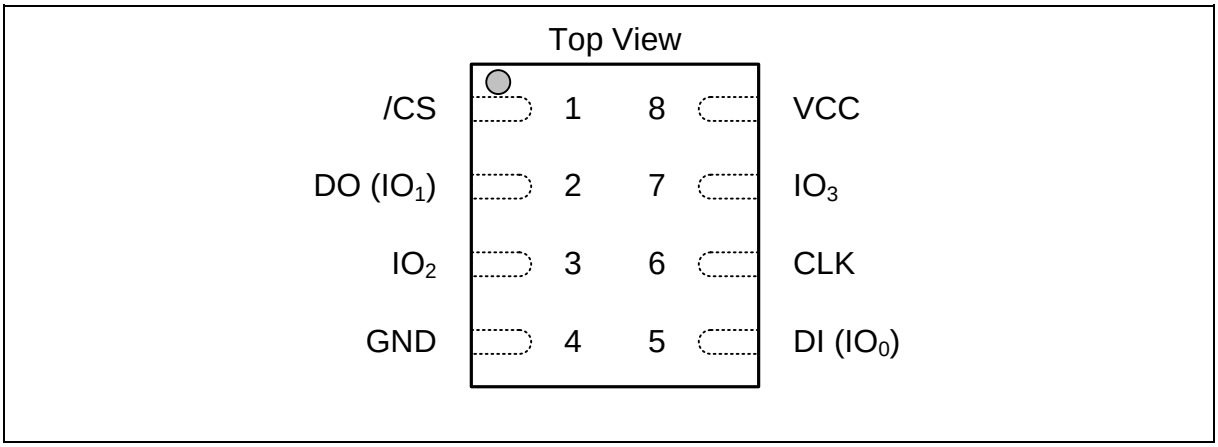


Figure 1. W25M121AV Pad Assignments, 8-pad WSON 8x6-mm (Package Code E)

3.2 Pad Description WSON 8x6-mm

PAD NO.	PAD NAME	I/O	FUNCTION
1	/CS	I	Chip Select Input
2	DO (IO1)	I/O	Data Output (Data Input Output 1)(1)
3	IO2	I/O	Data Input Output 2(2,3)
4	GND		Ground
5	DI (IO0)	I/O	Data Input (Data Input Output 0)(1)
6	CLK	I	Serial Clock Input
7	IO3	I/O	Data Input Output 3(2,3)
8	VCC		Power Supply

Notes:

1. IO0 and IO1 are used for Standard and Dual SPI instructions.
2. IO0 – IO3 are used for Quad SPI instructions.
3. For W25N01GV device in SPI / Dual SPI mode:
   - IO2 is a /WP pin.
   - IO3 is a /HOLD pin.

See appended W25N01GV data sheet for details.

4. DEVICE CONFIGURATION & PIN DESCRIPTIONS

4.1 Serial MCP (SpiStack®) Device Configuration

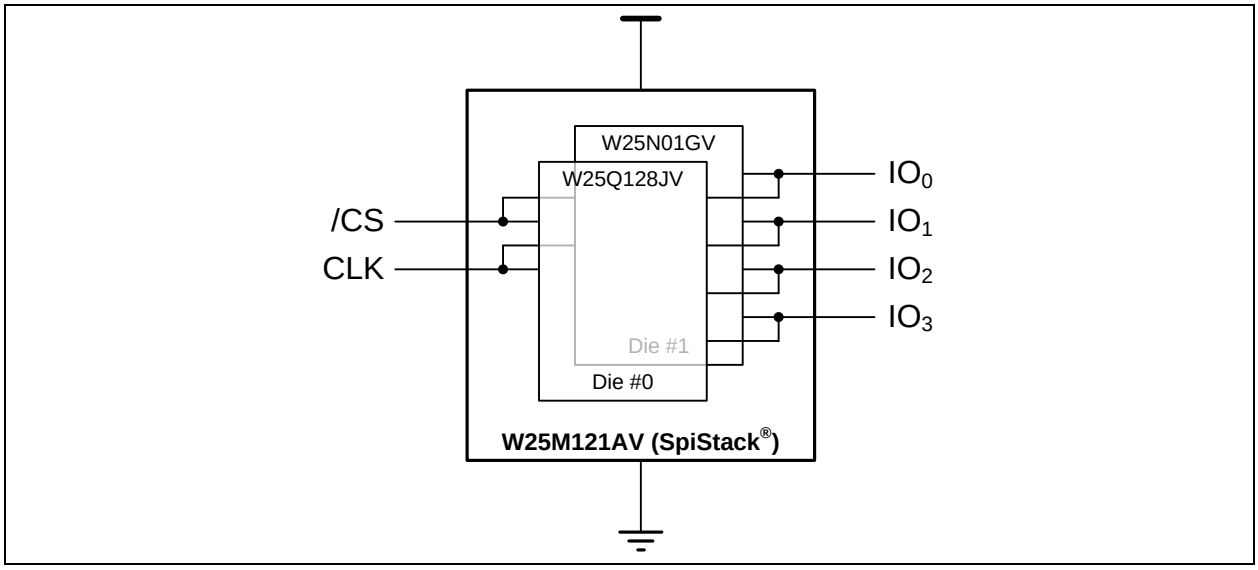


Figure 2. W25M121AV Device Configuration

All signal pins are shared by the stacked dice within the package. Each die is assigned a “Die ID#” in the factory. With the W25M121AV SpiStack® product, W25Q128JV die is factory assigned Die ID# 00h, while W25N01GV die is factory assigned Die ID# 01h. Only a single die is active at any given time, and have the control of the SPI bus to communicate with the external SPI controller. However, all the dice will accept “Software Die Select (C2h)” instruction and different software reset instruction regardless of their Active or Idle status. This universal “Software Die Select (C2h)” instruction is used to set any single die to be active according to the 8-bit Die ID following the instruction. Additionally, the two dice can also each accept different software reset instructions to reset each die to their power up state: 1) W25Q128JV can accept ”Software Reset (66h + 99h)” instruction sequence. 2) W25N01GV can accept “Device Reset (FFh) instruction.

4.2 Chip Select (/CS)

The SPI Chip Select (/CS) pin enables and disables device operation. When /CS is high the device is deselected and the Serial Data Output (DO, or IO0, IO1, IO2, IO3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When /CS is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, /CS must transition from high to low before a new instruction will be accepted. The /CS input must track the VCC supply level at power-up and power-down. If needed, a pull-up resistor on the /CS pin can be used to accomplish this.

4.3 Serial Input & Output (DI, DO and IO0, IO1, IO2, IO3)

The W25M121AV supports Standard SPI, Dual SPI and Quad SPI operation in each individual stacked die. All 8-bit instructions are shifted into the device through DI (IO0) pin, address and data are shifted in and out of the device through either DI & DO pins for Standard SPI instructions, IO0 & IO1 pins for Dual SPI instructions, or IO0-IO3 pins for Quad SPI instructions.

When W25N01GV die is selected and accessed in SPI or Dual SPI modes, the IO2 and IO3 pins will have /WP and /HOLD pins functionality, respectively. If the /HOLD pin functionality on IO3 is not used, IO3 should be driven high, so the W25N01GV device can respond to valid SPI and Dual SPI commands. If /HOLD pin is driven low (and /CS is low), the W25N01GV device is placed on a hold condition where the CLK, IO0 and IO1 signals will be gated off (active hold). If the /WP functionality is also not used, it is recommended that IO3 should also be driven high. /WP pin functionality on the W25N01GV device is used to protect against inadvertent writes to the Status Register. For details on /WP and /HOLD functionality, refer to the appended W25N01GV data sheet.

4.4 Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations.

5. CONCURRENT OPERATION DESCRIPTIONS

Once the device is power on, Die #0 will be active and have control of the SPI bus. “Software Die Select (C2h)” instruction followed by the 8-bit Die ID can be used to select the active die. The active die is available to accept any instruction issued by the controller and perform specific operations. The inactive/idle die does not accept any other instructions except the “Software Die Select (C2h)” instruction. However, the inactive/idle die can still perform internal Program/Erase operation which was initiated when the die was active. Therefore, “Read (on Active die) while Program/Erase (on Idle die)” and “Multi-die Program/Erase (both Active & Idle dice)” concurrent operations are feasible in the ***SpiStack***® series. “Software Die Select (C2h)” instruction will only change the active/idle status of the stacked dice, and it will not interrupt any on-going Program/Erase operations.

OPERATIONS	DIE #0 (W25Q128JV)	DIE #1 (W25N01GV)
Die #0 Active	Read/Program/Erase	Idle
Die #1 Active	Idle	Read/Program/Erase
Read while Program/Erase	Read (Active, uses SPI bus)	Program/Erase (Internal timing, no bus transaction)
	Program/Erase (Internal timing, no bus transaction)	Read (Active, uses SPI bus)
Multi-Die Program/Erase	Program/Erase (Internal timing, no bus transaction)	Program/Erase (Internal timing, no bus transaction)

Serial NOR and serial NAND comparison:

	DIE #0 (W25Q128JV)	DIE #1 (W25N01GV)
Density	128M-bit	1G-bit
Technology	NOR	SLC NAND
Endurance	100K cycles	100K cycles (with 1-bit ECC)
Max. Frequency	104MHz	104MHz
Read Throughput	52MB/s (Continuous)	52MB/s (Continuous Mode) 31.5MB/s (Buffer Mode)
Prog. Throughput	0.6MB/s	6.9MB/s
Erase Throughput	0.4MB/s (Block Erase)	64MB/s (Block Erase)

6. SOFTWARE DIE SELECT (C2H) INSTRUCTION

Each stacked die has a pre-assigned “Die ID#” by the factory, in the sequence of 0x00, 0x01, etc. At any given time, there can only be one Active Die within the W25M package, to communicate with the external SPI controller. After power-up, Die #0 is always the Active Die. Software Die Select (C2h) instruction is used to select a specific die to be active, according to the 8-bit Die ID following the C2h instruction as illustrated in Figure 3.

“Concurrent Operations” can be realized by assigning the current Active Die to perform an Erase/Program operation which requires some amount of time to finish. While the internal Program/Erase operation is on-going, the controller can issue a “Software Die Select (C2h)” instruction to select another die to be active. Depending on the system requirement, a Read, Program or Erase operation can be performed on the newly selected Active Die. “Read while Program/Erase” or “Multi-Die Program/Erase” can be performed in such fashion, to improve system Program/Erase throughput and to avoid constant Program/Erase Suspend and Resume activities in certain applications.

During the device Power-up and Reset time period, it is recommended not to issue “Software Die Select (C2h)” command to avoid the possible unknown state of the devices. Minimum tVSL (refer to individual datasheet) and maximum tRST (refer to individual datasheet) values can be applied to “Software Die Select (C2h)” command respectively.

In case of a wrong Die ID is sent to the device, both of the stacked dice may become idle. In such case, a new “Software Die Select (C2h)” command should be issued followed by a correct Die ID (00h or 01h) to re-select the Active Die.

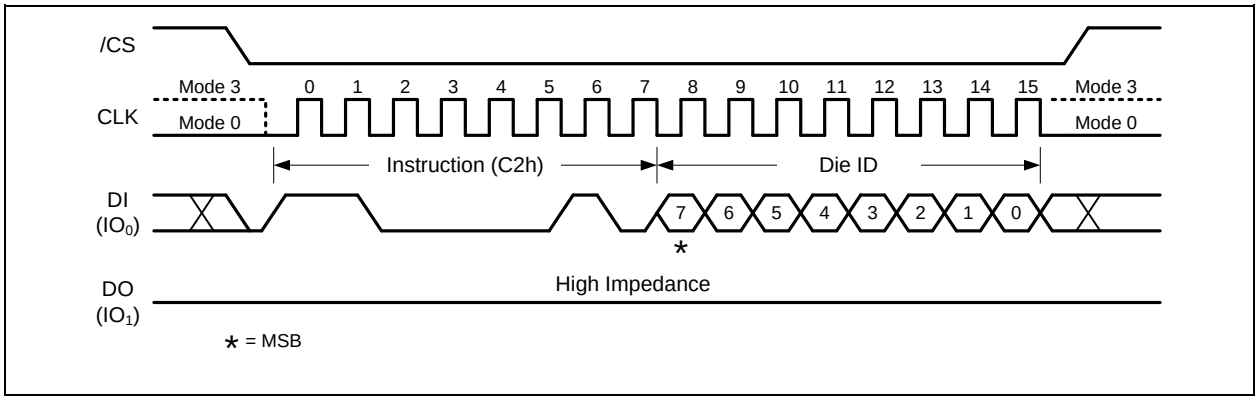


Figure 4. Software Die Select Instruction

7. SOFTWARE RESET

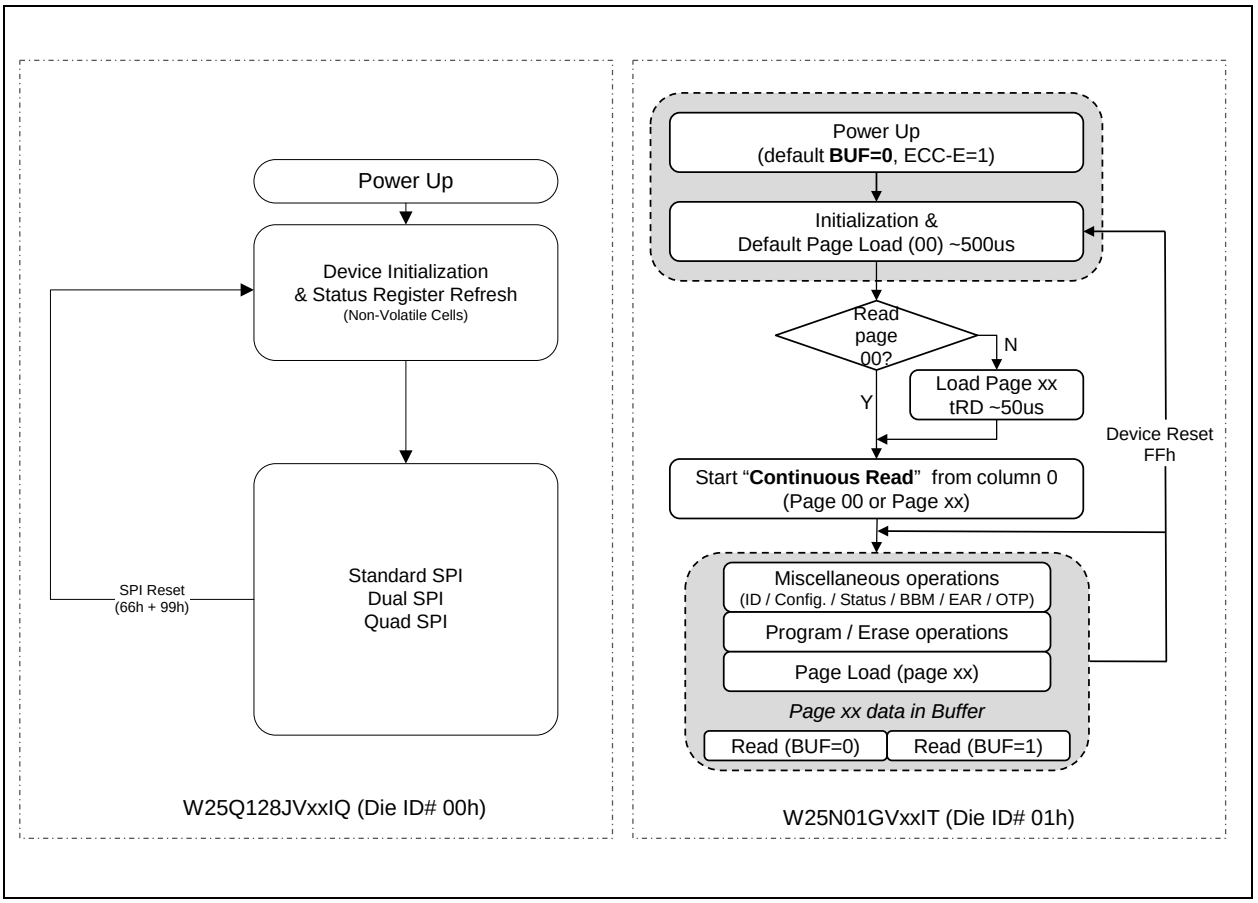


Figure 5. W25M121AV Software Reset Operation Flow

The W25M121AV device supports two different software Reset instruction for each die instead of a dedicated RESET pin due to the limitation of its 8-pin count small packages. Although only a single die is active and have the control of the SPI bus to communicate with the external SPI controller at any given time, the dice will be able to accept the valid software reset instruction despite their Active or Idle status.

The W25Q128JV die accepts Enable Reset (66h) and Reset (99h) instruction sequence while the W25N01GV die accepts Reset Device (FFh) instruction. When the device acknowledges the Reset instruction, any on-going internal operations will be terminated and the devices will return to its default power-on state and lose all the current volatile settings.

Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the BUSY bit and the SUS bit in Status Register before issuing the Reset command sequence.

Do not issue "Software Die Select (C2h)" during the tRST maximum time of either of the W25Q128JV die, which is 30us, or W25N01GV die, which is 500us, to prevent a possible die selection failure. For more details on software Reset functionality, refer to the appended W25Q128JV and W25N01GV data sheets.

7.1.1 *Enable Reset (66h) and Reset Device (99h)*

"Enable Reset (66h)" and "Reset (99h)" instructions can be issued in SPI mode to reset the W25Q128JV die to its default power on state. To avoid accidental reset, both instructions must be issued in sequence. Any other commands other than "Reset (99h)" after the "Enable Reset (66h)" command will disable the "Reset Enable" state. A new sequence of "Enable Reset (66h)" and "Reset (99h)" is needed to reset the device. Once the Reset command is accepted by the device, the device will take approximately tRST=30us to reset. During this period, no command will be accepted.

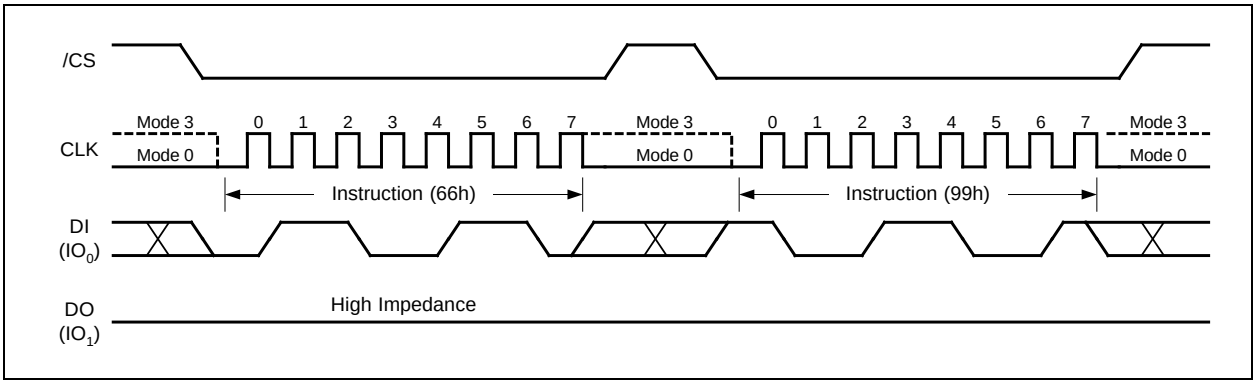


Figure 6. Enable Reset and Reset Instruction Sequence

7.1.2 Device Reset (FFh)

The Device Reset instruction (Figure 7) resets the W25N01GV die to its default power on state. The Device Reset instruction is entered by driving /CS low, shifting the instruction code "FFh" into the Data Input (DI) pin on the rising edge of CLK, and then driving /CS high. Once the Reset command is accepted, the W25N01GV die will take approximately tRST to reset. The reset period depends on the current operation being performed and tRST can be from 5us to 500us. During this period, no command will be accepted.

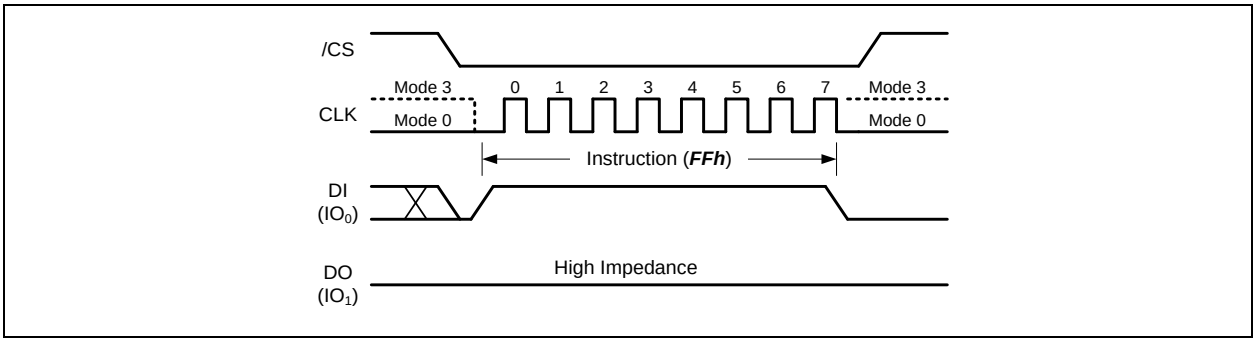
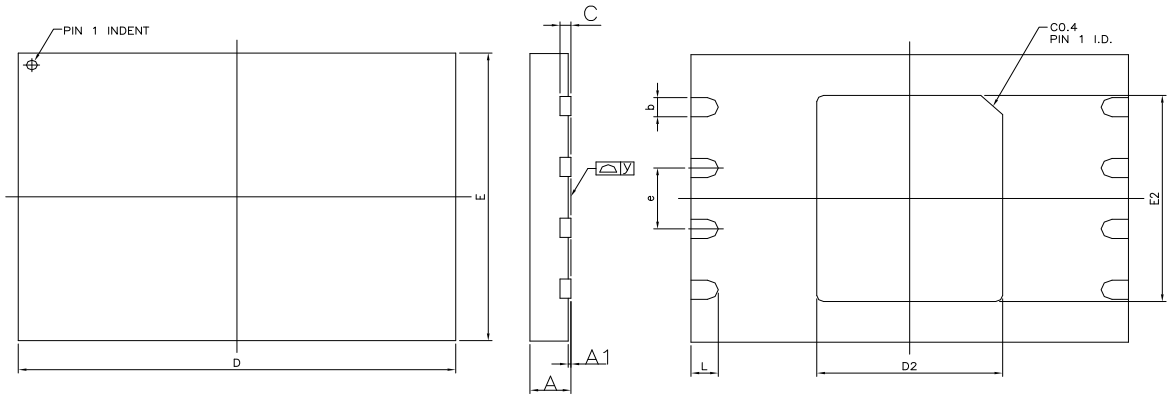


Figure 7. Device Reset Instruction

8. PACKAGE SPECIFICATIONS

8.1 8-Pad WSON 8x6-mm (Package Code E)



Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.35	0.40	0.48	0.014	0.016	0.019
C	---	0.20 REF	---	---	0.008 REF	---
D	7.90	8.00	8.10	0.311	0.315	0.319
D2	3.35	3.40	3.45	0.132	0.134	0.136
E	5.90	6.00	6.10	0.232	0.236	0.240
E2	4.25	4.30	4.35	0.167	0.169	0.171
e	---	1.27	---	---	0.050	---
L	0.45	0.50	0.55	0.018	0.020	0.022
y	0.00	---	0.050	0.000	---	0.002

9. ORDERING INFORMATION

W(1) 25M 121A V x I(1) x

Company Prefix

W = Winbond

Product Family

25M = Serial MCP SpiFlash Memory with SpiStack

Die ID Assignment / Memory Densities / Revision

121A = 128M-bit W25Q128JVxxIQ + 1G-bit W25N01GVxxIT

12: Die ID 0x00, 128Mb W25Q**128**JVxxIQ (Active from power-up)

1: Die ID 0x01, 1Gb W25N0**1**GVxxIT

Supply Voltage

V = 2.7V to 3.6V

Package Type

E = 8-pad WSON 8x6mm

Temperature Range

I = Industrial (-40°C to +85°C)

Special Options (2, 3)

T = Green Package (Lead-free, RoHS Compliant, Halogen-free (TBBA), Antimony-Oxide-free Sb_2O_3), W25N01GV default from power is BUF=0 (Continuous Read Mode), and W25Q128JV is Quad preset with QE bit = 1 of Status Register-2

Notes:

1. The “W” prefix is not included on the part marking.
2. Die configurations identifier of the SpiStack device.
3. Standard bulk shipments are in tray for WSON and package. For other packing options, please specify when placing orders.

9.1 Valid Part Numbers and Top Side Marking

The following table provides the valid part numbers for the W25M121AV SpiFlash Memory. Please contact Winbond for specific availability by density and package type. Winbond SpiFlash memories use a 12-digit Product Number for ordering. However, due to limited space, the Top Side Marking on all packages uses an abbreviated 11-digit number.

Industrial Temperature:

PACKAGE TYPE	DENSITY	PRODUCT NUMBER	TOP SIDE MARKING
ZE WSON-8 8x6mm	128M-bit + 1G-bit	W25M121AVEIT	25M121AVEIT

Note:
On W25N01GV die, BUF=0 (Continuous Read Mode) is the default value after power up. BUF bit can be written to 1.

10. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A	08/21/2017		New Create Preliminary

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W25Q128JVxIQ

Featuring

3V 128M-BIT
SERIAL FLASH MEMORY WITH
DUAL/QUAD SPI

Publication Release Date: August 23, 2017
Revision C

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1. GENERAL DESCRIPTIONS

The W25Q128JV (128M-bit) Serial Flash memory provides a storage solution for systems with limited space, pins and power. The 25Q series offers flexibility and performance well beyond ordinary Serial Flash devices. They are ideal for code shadowing to RAM, executing code directly from Dual/Quad SPI (XIP) and storing voice, text and data. The device operates on a single 2.7V to 3.6V power supply with current consumption as low as 1µA for power-down. All devices are offered in space-saving packages.

The W25Q128JV array is organized into 65,536 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time. Pages can be erased in groups of 16 (4KB sector erase), groups of 128 (32KB block erase), groups of 256 (64KB block erase) or the entire chip (chip erase). The W25Q128JV has 4,096 erasable sectors and 256 erasable blocks respectively. The small 4KB sectors allow for greater flexibility in applications that require data and parameter storage. (See Figure 1.)

The W25Q128JV supports the standard Serial Peripheral Interface (SPI), Dual/Quad I/O SPI: Serial Clock, Chip Select, Serial Data I/O0 (DI), I/O1 (DO), I/O2 and I/O3. SPI clock frequencies of W25Q128JV of up to 133MHz are supported allowing equivalent clock rates of 266MHz (133MHz x 2) for Dual I/O and 532MHz (133MHz x 4) for Quad I/O when using the Fast Read Dual/Quad I/O. These transfer rates can outperform standard Asynchronous 8 and 16-bit Parallel Flash memories.

Additionally, the device supports JEDEC standard manufacturer and device ID and SFDP, and a 64-bit Unique Serial Number and three 256-bytes Security Registers.

2. FEATURES

- **New Family of SpiFlash Memories**
  - W25Q128JV: 128M-bit / 16M-byte
  - Standard SPI: CLK, /CS, DI, DO
  - Dual SPI: CLK, /CS, IO_0, IO_1
  - Quad SPI: CLK, /CS, IO_0, IO_1, IO_2, IO_3
  - Software Reset
- **Highest Performance Serial Flash**
  - 133MHz Single, Dual/Quad SPI clocks
  - 266/532MHz equivalent Dual/Quad SPI
  - 66MB/S continuous data transfer rate
  - Min. 100K Program-Erase cycles per sector
  - More than 20-year data retention
- **Efficient "Continuous Read"**
  - Continuous Read with 8/16/32/64-Byte Wrap
  - As few as 8 clocks to address memory
  - Allows true XIP (execute in place) operation
  - Outperforms X16 Parallel Flash
- **Low Power, Wide Temperature Range**
  - Single 2.7V to 3.6V supply
  - <1µA Power-down (typ.)
  - -40°C to +85°C operating range
- **Flexible Architecture with 4KB sectors**
  - Uniform Sector/Block Erase (4K/32K/64K-Byte)
  - Program 1 to 256 byte per programmable page
  - Erase/Program Suspend & Resume
- **Advanced Security Features**
  - Software Write-Protect
  - Special OTP protection
  - Top/Bottom, Complement array protection
  - Individual Block/Sector array protection
  - 64-Bit Unique ID for each device
  - Discoverable Parameters (SFDP) Register
  - 3X256-Bytes Security Registers
  - Volatile & Non-volatile Status Register Bits

3. PIN DESCRIPTIONS

3.1 Chip Select (/CS)

The SPI Chip Select (/CS) pin enables and disables device operation. When /CS is high the device is deselected and the Serial Data Output (DO, or IO0, IO1, IO2, IO3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When /CS is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, /CS must transition from high to low before a new instruction will be accepted. The /CS input must track the VCC supply level at power-up and power-down (see “Write Protection” and Figure 41). If needed a pull-up resister on the /CS pin can be used to accomplish this.

3.2 Serial Data Input, Output and IOs (DI, DO and IO0, IO1, IO2, IO3)

The W25Q128JV supports Standard SPI, Dual SPI and Quad SPI operation in each individual stacked die. All 8-bit instructions are shifted into the device through DI (IO0) pin, address and data are shifted in and out of the device through either DI & DO pins for Standard SPI instructions, IO0 & IO1 pins for Dual SPI instructions, or IO0-IO3 pins for Quad SPI instructions.

3.3 Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Operations")

4. BLOCK DIAGRAM

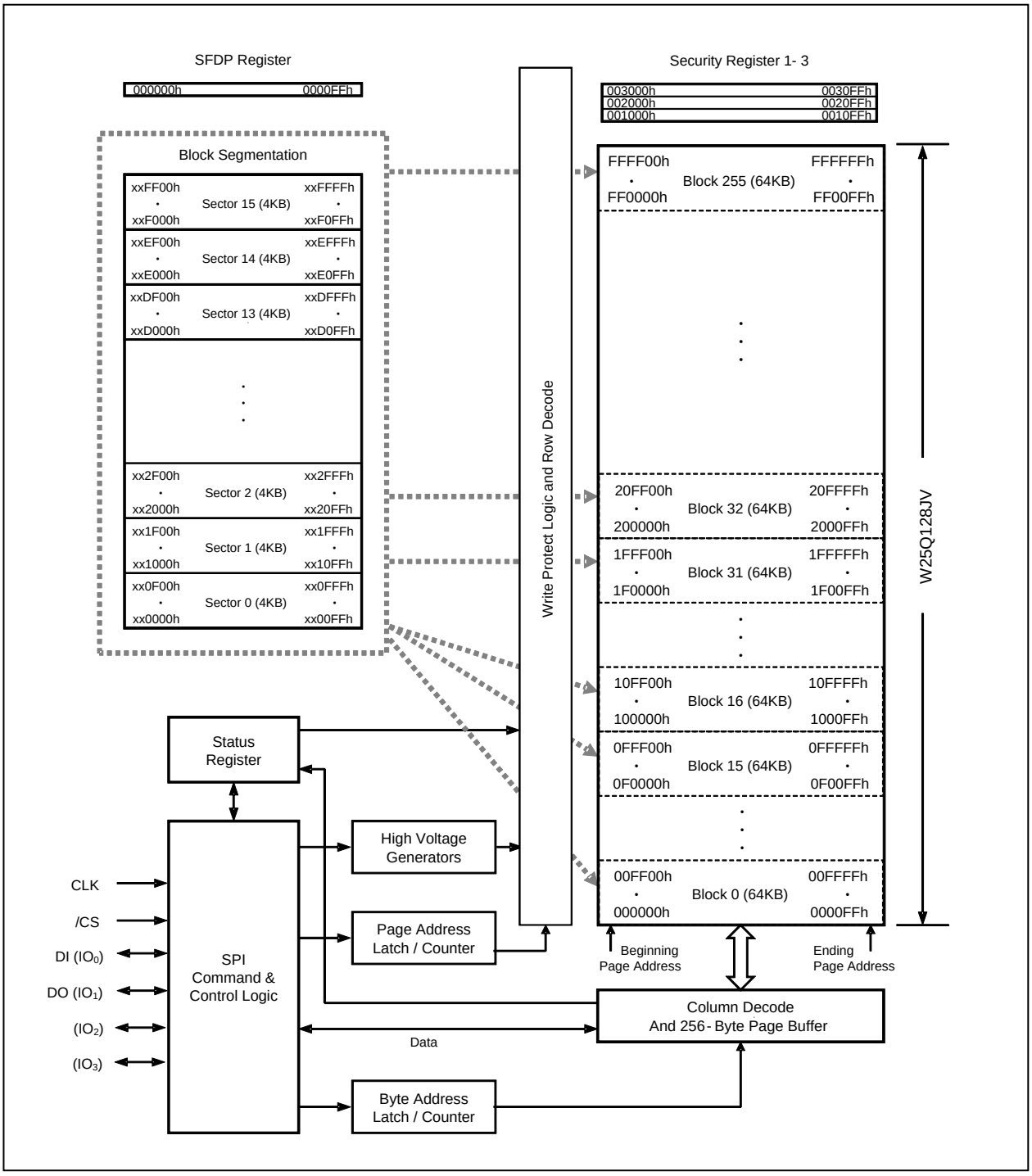


Figure 1. W25Q128JV Serial Flash Memory Block Diagram

5. FUNCTIONAL DESCRIPTIONS

5.1 Standard SPI Instructions

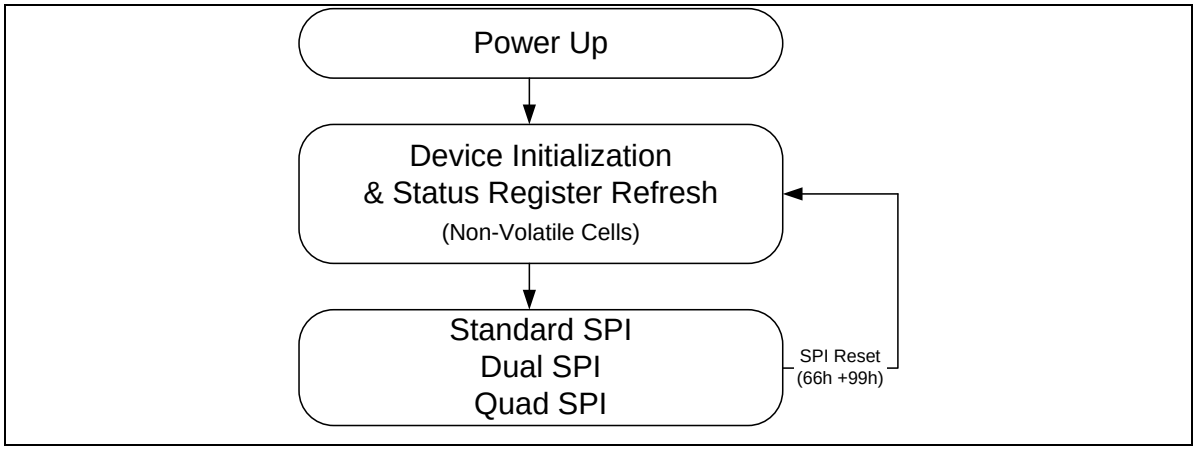


Figure 2. W25Q128JV Serial Flash Memory Operation Diagram

The W25Q128JV is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (/CS), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge of CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of /CS. For Mode 3, the CLK signal is normally high on the falling and rising edges of /CS.

5.1.1 Dual SPI Instructions

The W25Q128JV supports Dual SPI operation when using instructions such as “Fast Read Dual Output (3Bh)” and “Fast Read Dual I/O (BBh)”. These instructions allow data to be transferred to or from the device at two to three times the rate of ordinary Serial Flash devices. The Dual SPI Read instructions are ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed-critical code directly from the SPI bus (XIP). When using Dual SPI instructions, the DI and DO pins become bidirectional I/O pins: IO0 and IO1.

5.1.2 Quad SPI Instructions

The W25Q128JV supports Quad SPI operation when using instructions such as “Fast Read Quad Output (6Bh)”, and “Fast Read Quad I/O (EBh). These instructions allow data to be transferred to or from the device four to six times the rate of ordinary Serial Flash. The Quad Read instructions offer a significant improvement in continuous and random access transfer rates allowing fast code-shadowing to RAM or execution directly from the SPI bus (XIP). When using Quad SPI instructions the DI and DO pins become bidirectional IO0 and IO1, with the additional I/O pins: IO2, IO3.

5.1.3 Software Reset

The W25Q128JV can be reset to the initial power-on state by a software Reset sequence. This sequence must include two consecutive instructions: Enable Reset (66h) & Reset (99h). If the instruction sequence is successfully accepted, the device will take approximately 30µS (t_{RST}) to reset. No instruction will be accepted during the reset period.

5.2 Write Protection

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern, the W25Q128JV provides several means to protect the data from inadvertent writes.

5.2.1 Write Protect Features

- Device resets when VCC is below threshold
- Time delay write disable after Power-up
- Write enable/disable instructions and automatic write disable after erase or program
- Software write protection using Status Registers
- Additional Individual Block/Sector Locks for array protection
- Write Protection using Power-down instruction
- Lock Down write protection for Status Register until the next power-up
- One Time Program (OTP) write protection for array and Security Registers using Status Register*

  * Note: This feature is available upon special order. Please contact Winbond for details.

Upon power-up or at power-down, the W25Q128JV will maintain a reset condition while VCC is below the threshold value of V_{WI}, (See Power-up Timing and Voltage Levels and Figure 41). While reset, all operations are disabled and no instructions are recognized. During power-up and after the VCC voltage exceeds V_{WI}, all program and erase related instructions are further disabled for a time delay of t_{PUW}. This includes the Write Enable, Page Program, Sector Erase, Block Erase, Chip Erase and the Write Status Register instructions. Note that the chip select pin (/CS) must track the VCC supply level at power-up until the VCC-min level and t_{VSL} time delay is reached, and it must also track the VCC supply level at power-down to prevent adverse command sequence. If needed a pull-up resister on /CS can be used to accomplish this.

After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a Page Program, Sector Erase, Block Erase, Chip Erase or Write Status Register instruction will be accepted. After completing a program, erase or write instruction the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (SRL) and Block Protect (CMP, SEC, TB, BP[2:0]) bits. These settings allow a portion or the entire memory array to be configured as read only.

The W25Q128JV also provides another Write Protect method using the Individual Block Locks. Each 64KB block (except the top and bottom blocks, total of 126 blocks) and each 4KB sector within the top/bottom blocks (total of 32 sectors) are equipped with an Individual Block Lock bit. When the lock bit is 0, the corresponding sector or block can be erased or programmed; when the lock bit is set to 1, Erase or Program commands issued to the corresponding sector or block will be ignored. When the device is powered on, all Individual Block Lock bits will be 1, so the entire memory array is protected from Erase/Program. An “Individual Block Unlock (39h)” instruction must be issued to unlock any specific sector or block.

The WPS bit in Status Register-3 is used to decide which Write Protect scheme should be used. When WPS=0 (factory default), the device will only utilize CMP, SEC, TB, BP[2:0] bits to protect specific areas of the array; when WPS=1, the device will utilize the Individual Block Locks for write protection.

6. STATUS AND CONFIGURATION REGISTERS

Three Status and Configuration Registers are provided for W25Q128JV. The Read Status Register-1/2/3 instructions can be used to provide status on the availability of the flash memory array, whether the device is write enabled or disabled, the state of write protection, Quad SPI setting, Security Register lock status, Erase/Program Suspend status, output driver strength, power-up. The Write Status Register instruction can be used to configure the device write protection features, Quad SPI setting, Security Register OTP locks, and output driver strength. Write access to the Status Register is controlled by the state of the non-volatile Status Register Protect bits (SRL), the Write Enable instruction, and during Standard/Dual SPI operations

6.1 Status Registers

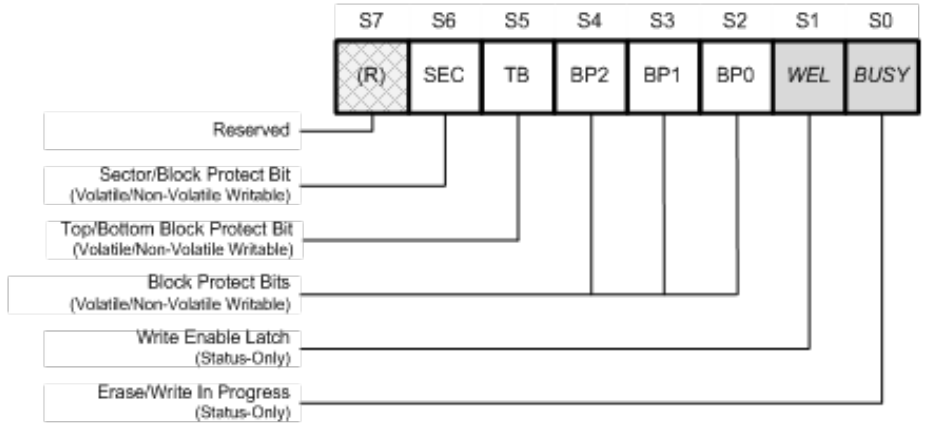


Figure 3a. Status Register-1

6.1.1 Erase/Write In Progress (BUSY) – *Status Only*

BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is executing a Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register or Erase/Program Security Register instruction. During this time the device will ignore further instructions except for the Read Status Register and Erase/Program Suspend instruction (see t_W, t_{PP}, t_{SE}, t_{BE}, and t_{CE} in AC Characteristics). When the program, erase or write status/security register instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions.

6.1.2 Write Enable Latch (WEL) – *Status Only*

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to 1 after executing a Write Enable Instruction. The WEL status bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Erase Security Register and Program Security Register.

6.1.3 Block Protect Bits (BP2, BP1, BP0) – *Volatile/Non-Volatile Writable*

The Block Protect Bits (BP2, BP1, BP0) are non-volatile read/write bits in the status register (S4, S3, and S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction (see t_W in AC characteristics). All, none or a portion of the memory array can be

protected from Program and Erase instructions (see Status Register Memory Protection table). The factory default setting for the Block Protection Bits is 0, none of the array protected.

6.1.4 Top/Bottom Block Protect (TB) – *Volatile/Non-Volatile Writable*

The non-volatile Top/Bottom bit (TB) controls if the Block Protect Bits (BP2, BP1, BP0) protect from the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The factory default setting is TB=0. The TB bit can be set with the Write Status Register Instruction depending on the state of the SRP, SRL and WEL bits.

6.1.5 Sector/Block Protect Bit (SEC) – *Volatile/Non-Volatile Writable*

The non-volatile Sector/Block Protect bit (SEC) controls if the Block Protect Bits (BP2, BP1, BP0) protect either 4KB Sectors (SEC=1) or 64KB Blocks (SEC=0) in the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The default setting is SEC=0.

6.1.6 Complement Protect (CMP) – *Volatile/Non-Volatile Writable*

The Complement Protect bit (CMP) is a non-volatile read/write bit in the status register (S14). It is used in conjunction with SEC, TB, BP2, BP1 and BP0 bits to provide more flexibility for the array protection. Once CMP is set to 1, previous array protection set by SEC, TB, BP2, BP1 and BP0 will be reversed. For instance, when CMP=0, a top 64KB block can be protected while the rest of the array is not; when CMP=1, the top 64KB block will become unprotected while the rest of the array become read-only. Please refer to the Status Register Memory Protection table for details. The default setting is CMP=0.

6.1.7 Status Register Protect (SRL)

The Status Register Lock bit (SRL) is a volatile/non-volatile read/write bit in the status register (S8). The SRL bit controls the method of write protection to the Status Registers: temporary Power Lock-Down or permanently One Time Program OTP.

SRL	Status Register Lock	Description
0	Non-Lock	Status Registers are unlocked.
1	Power Lock-Down (Temporary/Volatile)	Status Registers are locked and cannot be written to until the next power-down, power-up cycle to reset SRL=0.
	One Time Program(1) (Permanently/Non-Volatile)	A special instruction flow can be used to permanently OTP lock the Status Registers.

Note: Please contact Winbond for details regarding the special instruction sequence.

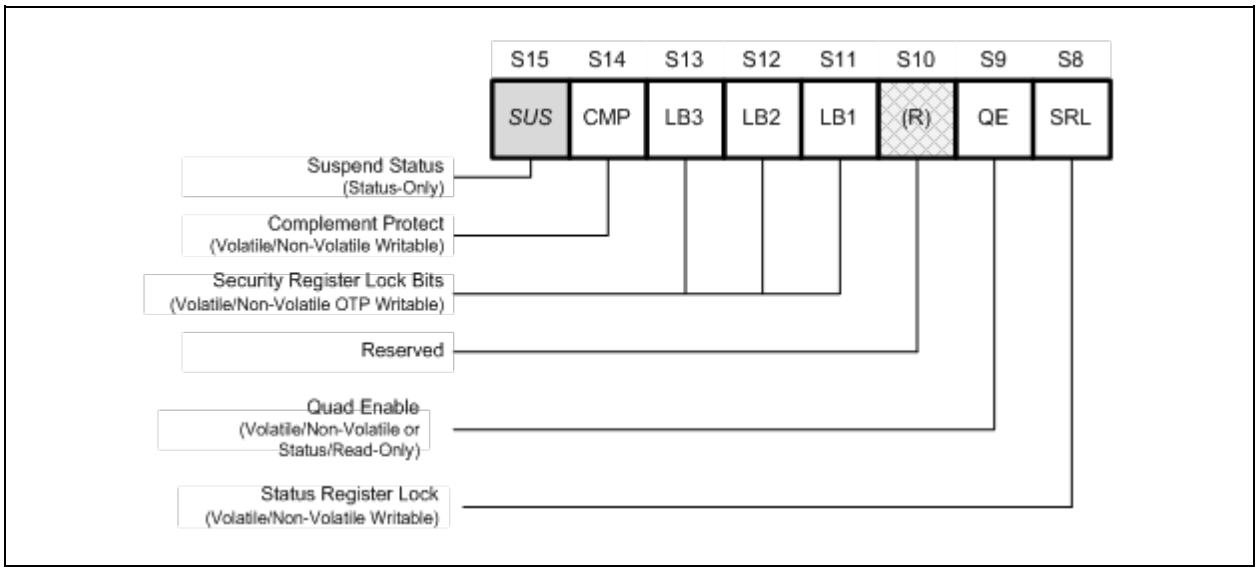


Figure 3b. Status Register-2

6.1.8 Erase/Program Suspend Status (SUS) – *Status Only*

The Suspend Status bit is a read only bit in the status register (S15) that is set to 1 after executing a Erase/Program Suspend (75h) instruction. The SUS status bit is cleared to 0 by Erase/Program Resume (7Ah) instruction as well as a power-down, power-up cycle.

6.1.9 Security Register Lock Bits (LB3, LB2, LB1) – *Volatile/Non-Volatile OTP Writable*

The Security Register Lock Bits (LB3, LB2, LB1) are non-volatile One Time Program (OTP) bits in Status Register (S13, S12, S11) that provide the write protect control and status to the Security Registers. The default state of LB3-1 is 0, Security Registers are unlocked. LB3-1 can be set to 1 individually using the Write Status Register instruction. LB3-1 are One Time Programmable (OTP), once it's set to 1, the corresponding 256-Byte Security Register will become read-only permanently.

6.1.10 Quad Enable (QE) – *Volatile/Non-Volatile Writable* or Status/Read Only

The Quad Enable (QE) bit is a non-volatile read/write bit in the status register (S9) that allows Quad SPI operation. When the QE bit is set to a 0 state (factory default for part numbers with ordering options "IM"). In this configuration, the /WP pin and /HOLD are enabled.

When the QE bit is set to a '1' (factory default for Quad Enabled part numbers with ordering option "IQ"), the Quad IO2 and IO3 pins are enabled, and /WP and /HOLD functions are disabled In this configuration, the Quad Enable (QE) bit is a read only bit in the status register (S9) that allows Quad SPI operation.

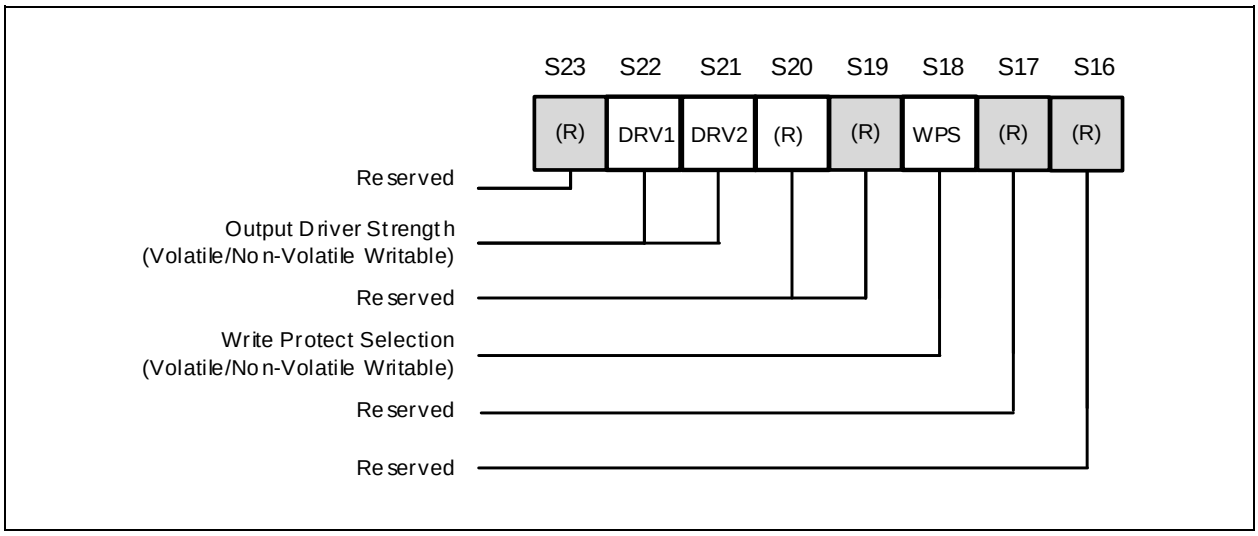


Figure 3c. Status Register-3

6.1.11 Write Protect Selection (WPS) – *Volatile/Non-Volatile Writable*

The WPS bit is used to select which Write Protect scheme should be used. When WPS=0, the device will use the combination of CMP, SEC, TB, BP[2:0] bits to protect a specific area of the memory array. When WPS=1, the device will utilize the Individual Block Locks to protect any individual sector or blocks. The default value for all Individual Block Lock bits is 1 upon device power on or after reset.

6.1.12 Output Driver Strength (DRV1, DRV0) – *Volatile/Non-Volatile Writable*

The DRV1 & DRV0 bits are used to determine the output driver strength for the Read operations.

DRV1, DRV0	Driver Strength
0, 0	100%
0, 1	75%
1, 0	50%
1, 1	25% (default)

6.1.13 Reserved Bits – *Non Functional*

There are a few reserved Status Register bits that may be read out as a “0” or “1”. It is recommended to ignore the values of those bits. During a “Write Status Register” instruction, the Reserved Bits can be written as “0”, but there will not be any effects.

6.1.14 W25Q128JV Status Register Memory Protection (WPS = 0, CMP = 0)

STATUS REGISTER[1]					W25Q128JV (128M-BIT) MEMORY PROTECTION[3]			
SEC	TB	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESSES	PROTECTED DENSITY	PROTECTED PORTION[2]
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	252 thru 255	FC0000h – FFFFFFh	256KB	Upper 1/64
0	0	0	1	0	248 thru 255	F80000h – FFFFFFh	512KB	Upper 1/32
0	0	0	1	1	240 thru 255	F00000h – FFFFFFh	1MB	Upper 1/16
0	0	1	0	0	224 thru 255	E00000h – FFFFFFh	2MB	Upper 1/8
0	0	1	0	1	192 thru 255	C00000h – FFFFFFh	4MB	Upper 1/4
0	0	1	1	0	128 thru 255	800000h – FFFFFFh	8MB	Upper 1/2
0	1	0	0	1	0 thru 3	000000h – 03FFFFh	256KB	Lower 1/64
0	1	0	1	0	0 thru 7	000000h – 07FFFFh	512KB	Lower 1/32
0	1	0	1	1	0 thru 15	000000h – 0FFFFFh	1MB	Lower 1/16
0	1	1	0	0	0 thru 31	000000h – 1FFFFFh	2MB	Lower 1/8
0	1	1	0	1	0 thru 63	000000h – 3FFFFFh	4MB	Lower 1/4
0	1	1	1	0	0 thru 127	000000h – 7FFFFFh	8MB	Lower 1/2
X	X	1	1	1	0 thru 255	000000h – FFFFFFh	16MB	ALL
1	0	0	0	1	255	FFF000h – FFFFFFh	4KB	U - 1/4096
1	0	0	1	0	255	FFE000h – FFFFFFh	8KB	U - 1/2048
1	0	0	1	1	255	FFC000h – FFFFFFh	16KB	U - 1/1024
1	0	1	0	X	255	FF8000h – FFFFFFh	32KB	U - 1/512
1	1	0	0	1	0	000000h – 000FFFh	4KB	L - 1/4096
1	1	0	1	0	0	000000h – 001FFFh	8KB	L - 1/2048
1	1	0	1	1	0	000000h – 003FFFh	16KB	L - 1/1024
1	1	1	0	X	0	000000h – 007FFFh	32KB	L - 1/512

Notes:
1. X = don't care
2. L = Lower; U = Upper
3. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

6.1.15 W25Q128JV Status Register Memory Protection (WPS = 0, CMP = 1)

STATUS REGISTER[1]					W25Q128JV (128M-BIT) MEMORY PROTECTION[3]			
SEC	TB	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESSES	PROTECTED DENSITY	PROTECTED PORTION[2]
X	X	0	0	0	0 thru 255	000000h - FFFFFFh	16MB	ALL
0	0	0	0	1	0 thru 251	000000h - FBFFFFh	16,128KB	Lower 63/64
0	0	0	1	0	0 thru 247	000000h – F7FFFFh	15,872KB	Lower 31/32
0	0	0	1	1	0 thru 239	000000h - EFFFFFh	15MB	Lower 15/16
0	0	1	0	0	0 thru 223	000000h - DFFFFFh	14MB	Lower 7/8
0	0	1	0	1	0 thru 191	000000h - BFFFFFh	12MB	Lower 3/4
0	0	1	1	0	0 thru 127	000000h - 7FFFFFh	8MB	Lower 1/2
0	1	0	0	1	4 thru 255	040000h - FFFFFFh	16,128KB	Upper 63/64
0	1	0	1	0	8 thru 255	080000h - FFFFFFh	15,872KB	Upper 31/32
0	1	0	1	1	16 thru 255	100000h - FFFFFFh	15MB	Upper 15/16
0	1	1	0	0	32 thru 255	200000h - FFFFFFh	14MB	Upper 7/8
0	1	1	0	1	64 thru 255	400000h - FFFFFFh	12MB	Upper 3/4
0	1	1	1	0	128 thru 255	800000h - FFFFFFh	8MB	Upper 1/2
X	X	1	1	1	NONE	NONE	NONE	NONE
1	0	0	0	1	0 thru 255	000000h – FFEFFFh	16,380KB	L - 4095/4096
1	0	0	1	0	0 thru 255	000000h – FFDFFFh	16,376KB	L - 2047/2048
1	0	0	1	1	0 thru 255	000000h – FFBFFFh	16,368KB	L - 1023/1024
1	0	1	0	X	0 thru 255	000000h – FF7FFFh	16,352KB	L - 511/512
1	1	0	0	1	0 thru 255	001000h – FFFFFFh	16,380KB	U - 4095/4096
1	1	0	1	0	0 thru 255	002000h – FFFFFFh	16,376KB	U - 2047/2048
1	1	0	1	1	0 thru 255	004000h – FFFFFFh	16,368KB	U -1023/1024
1	1	1	0	X	0 thru 255	008000h – FFFFFFh	16,352KB	U - 511/512

Notes:
1. X = don't care
2. L = Lower; U = Upper
3. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

6.1.16 W25Q128JV Individual Block Memory Protection (WPS=1)

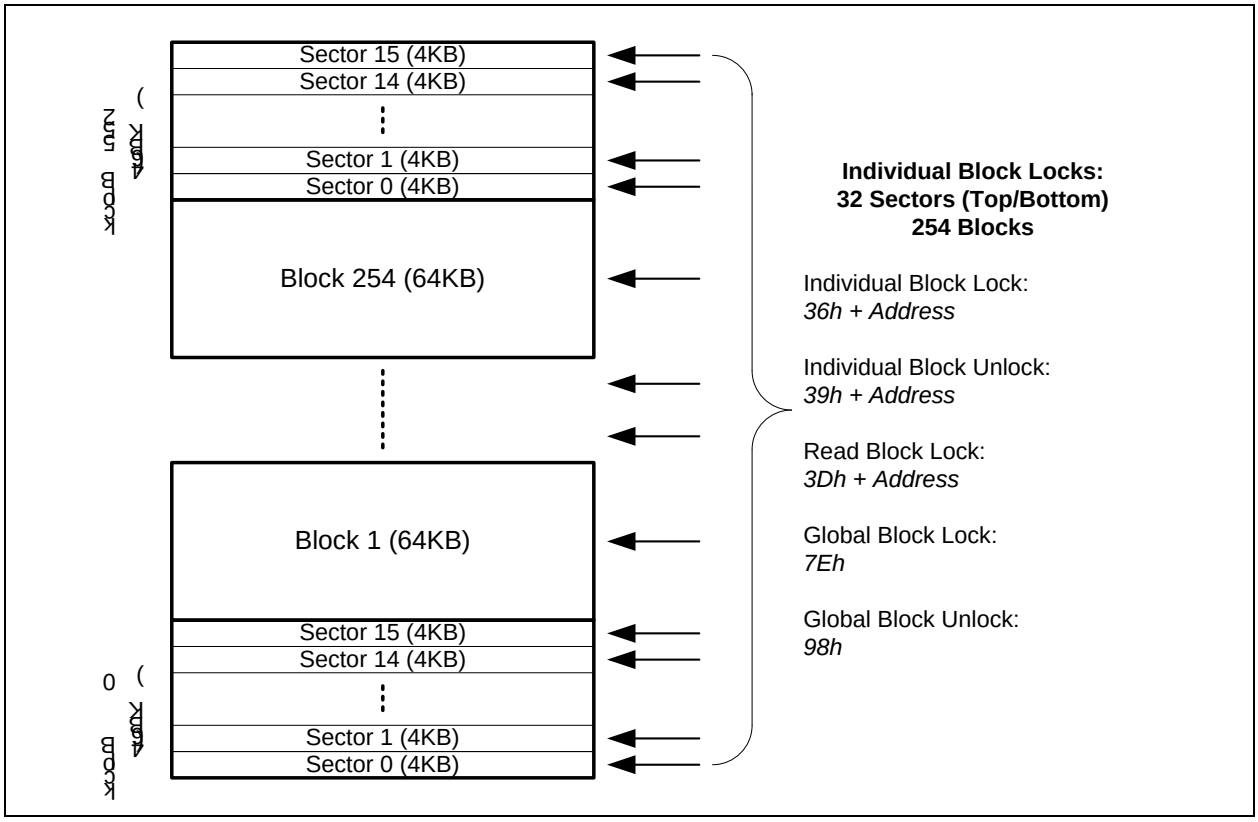


Figure 3d. Individual Block/Sector Locks

Notes:

1. Individual Block/Sector protection is only valid when WPS=1.
2. All individual block/sector lock bits are set to 1 by default after power up, all memory array is protected.

7. INSTRUCTIONS

The Standard/Dual/Quad SPI instruction set of the W25Q128JV consists of 48 basic instructions that are fully controlled through the SPI bus (see Instruction Set Table1-2). Instructions are initiated with the falling edge of Chip Select (/CS). The first byte of data clocked into the DI input provides the instruction code. Data on the DI input is sampled on the rising edge of clock with most significant bit (MSB) first.

Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don't care), and in some cases, a combination. Instructions are completed with the rising edge of edge /CS. Clock relative timing diagrams for each instruction are included in Figures 4 through 40. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte boundary (/CS driven high after a full 8-bits have been clocked) otherwise the instruction will be ignored. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all instructions except for Read Status Register will be ignored until the program or erase cycle has completed.

7.1 Device ID and Instruction Set Tables

7.1.1 Manufacturer and Device Identification

MANUFACTURER ID	**(MF7 - MF0)**	
Winbond Serial Flash	EFh	
Device ID	**(ID7 - ID0)**	**(ID15 - ID0)**
Instruction	**ABh, 90h, 92h, 94h**	**9Fh**
W25Q128JVxIQ SPISTACK	17h	4018h

7.1.2 Instruction Set Table 1 (Standard SPI Instructions)[1]

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Number of Clock(1-1-1)	**8**	**8**	**8**	**8**	**8**	**8**	**8**
Write Enable	**06h**						
Volatile SR Write Enable	**50h**						
Write Disable	**04h**						
Release Power-down / ID	**ABh**	Dummy	Dummy	Dummy	(ID7-ID0)[2]		
Manufacturer/Device ID	**90h**	Dummy	Dummy	00h	(MF7-MF0)	(ID7-ID0)	
JEDEC ID	**9Fh**	(MF7-MF0)	(ID15-ID8)	(ID7-ID0)			
Read Unique ID	**4Bh**	Dummy	Dummy	Dummy	Dummy	(UID63-0)	
Read Data	**03h**	A23-A16	A15-A8	A7-A0	(D7-D0)		
Fast Read	**0Bh**	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	
Page Program	**02h**	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0[3]	
Sector Erase (4KB)	**20h**	A23-A16	A15-A8	A7-A0			
Block Erase (32KB)	**52h**	A23-A16	A15-A8	A7-A0			
Block Erase (64KB)	**D8h**	A23-A16	A15-A8	A7-A0			
Chip Erase	**C7h/60h**						
Read Status Register-1	**05h**	(S7-S0)[2]					
Write Status Register-1[4]	**01h**	(S7-S0)[4]					
Read Status Register-2	**35h**	(S15-S8)[2]					
Write Status Register-2	**31h**	(S15-S8)					
Read Status Register-3	**15h**	(S23-S16)[2]					
Write Status Register-3	**11h**	(S23-S16)					
Read SFDP Register	**5Ah**	00	00	A7-A0	Dummy	(D7-D0)	
Erase Security Register[5]	**44h**	A23-A16	A15-A8	A7-A0			
Program Security Register[5]	**42h**	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0[3]	
Read Security Register[5]	**48h**	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	
Global Block Lock	**7Eh**						
Global Block Unlock	**98h**						
Read Block Lock	**3Dh**	A23-A16	A15-A8	A7-A0	(L7-L0)		
Individual Block Lock	**36h**	A23-A16	A15-A8	A7-A0			
Individual Block Unlock	**39h**	A23-A16	A15-A8	A7-A0			
Erase / Program Suspend	**75h**						
Erase / Program Resume	**7Ah**						
Power-down	**B9h**						
Enable Reset	**66h**						
Reset Device	**99h**						

7.1.3 Instruction Set Table 2 (Dual/Quad SPI Instructions)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9
Number of Clock(1-1-2)	**8**	**8**	**8**	**8**	**4**	**4**	**4**	**4**	**4**
Fast Read Dual Output	**3Bh**	A23-A16	A15-A8	A7-A0	Dummy	Dummy	(D7-D0)(7)		
Number of Clock(1-2-2)	**8**	**4**	**4**	**4**	**4**	**4**	**4**	**4**	**4**
Fast Read Dual I/O	**BBh**	A23-A16(6)	A15-A8(6)	A7-A0(6)	Dummy(11)	(D7-D0)(7)			
Mftr./Device ID Dual I/O	**92h**	A23-A16(6)	A15-A8(6)	00(6)	Dummy(11)	(MF7-MF0)	(ID7-ID0)(7)		
Number of Clock(1-1-4)	**8**	**8**	**8**	**8**	**2**	**2**	**2**	**2**	**2**
Quad Input Page Program	**32h**	A23-A16	A15-A8	A7-A0	(D7-D0)(9)	(D7-D0)(3)	…		
Fast Read Quad Output	**6Bh**	A23-A16	A15-A8	A7-A0	Dummy	Dummy	Dummy	Dummy	(D7-D0)(10)
Number of Clock(1-4-4)	**8**	**2**(8)	**2**(8)	**2**(8)	**2**	**2**	**2**	**2**	**2**
Mftr./Device ID Quad I/O	**94h**	A23-A16	A15-A8	00	Dummy(11)	Dummy	Dummy	(MF7-MF0)	(ID7-ID0)
Fast Read Quad I/O	**EBh**	A23-A16	A15-A8	A7-A0	Dummy(11)	Dummy	Dummy	(D7-D0)	
Set Burst with Wrap	**77h**	Dummy	Dummy	Dummy	W8-W0				

Notes:

1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis "( )" indicate data output from the device on either 1, 2 or 4 IO pins.
2. The Status Register contents and Device ID will repeat continuously until /CS terminates the instruction.
3. At least one byte of data input is required for Page Program, Quad Page Program and Program Security Registers, up to 256 bytes of data input. If more than 256 bytes of data are sent to the device, the addressing will wrap to the beginning of the page and overwrite previously sent data.
4. Write Status Register-1 (01h) can also be used to program Status Register-1&2, see section 7.2.5.
5. Security Register Address:
   Security Register 1: A23-16 = 00h; A15-8 = 10h; A7-0 = byte address
   Security Register 2: A23-16 = 00h; A15-8 = 20h; A7-0 = byte address
   Security Register 3: A23-16 = 00h; A15-8 = 30h; A7-0 = byte address
6. Dual SPI address input format:
   IO0 = A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0, M6, M4, M2, M0
   IO1 = A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1, M7, M5, M3, M1
7. Dual SPI data output format:
   IO0 = (D6, D4, D2, D0)
   IO1 = (D7, D5, D3, D1)
8. Quad SPI address input format:
   IO0 = A20, A16, A12, A8, A4, A0, M4, M0
   IO1 = A21, A17, A13, A9, A5, A1, M5, M1
   IO2 = A22, A18, A14, A10, A6, A2, M6, M2
   IO3 = A23, A19, A15, A11, A7, A3, M7, M3

   Set Burst with Wrap input format:
   IO0 = x, x, x, x, x, x, W4, x
   IO1 = x, x, x, x, x, x, W5, x
   IO2 = x, x, x, x, x, x, W6, x
   IO3 = x, x, x, x, x, x, x, x
9. Quad SPI data input/output format:
   IO0 = (D4, D0, …..)
   IO1 = (D5, D1, …..)
   IO2 = (D6, D2, …..)
   IO3 = (D7, D3, …..)
10. Fast Read Quad I/O data output format:
   IO0 = (x, x, x, x, D4, D0, D4, D0)
   IO1 = (x, x, x, x, D5, D1, D5, D1)
   IO2 = (x, x, x, x, D6, D2, D6, D2)
   IO3 = (x, x, x, x, D7, D3, D7, D3)

11. The first dummy is M7-M0 should be set to FFh

7.2 Instruction Descriptions

7.2.1 Write Enable (06h)

The Write Enable instruction (Figure 4) sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register and Erase/Program Security Registers instruction. The Write Enable instruction is entered by driving /CS low, shifting the instruction code “06h” into the Data Input (DI) pin on the rising edge of CLK, and then driving /CS high.

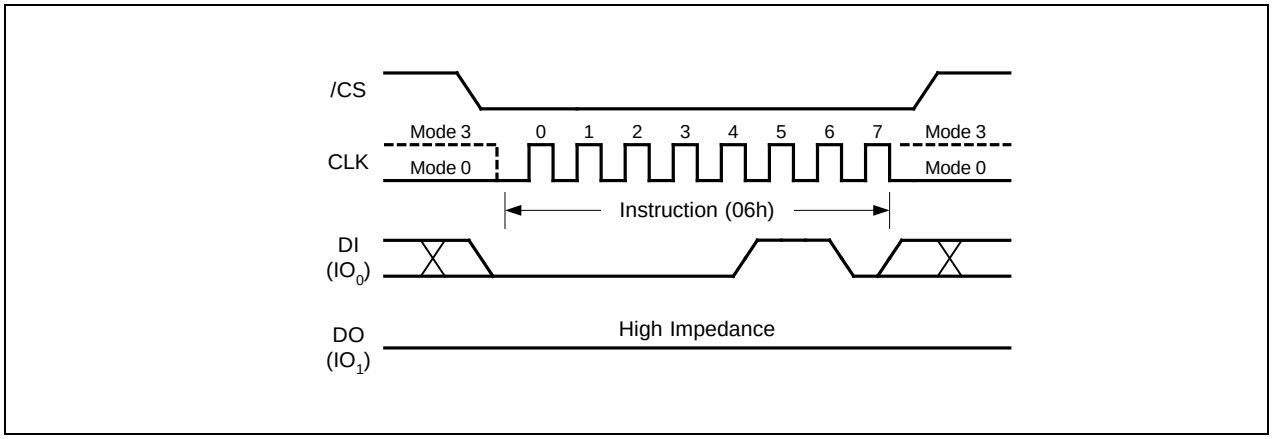


Figure 4. Write Enable Instruction for SPI Mode

7.2.2 Write Enable for Volatile Status Register (50h)

The non-volatile Status Register bits described in section 6.1 can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. To write the volatile values into the Status Register bits, the Write Enable for Volatile Status Register (50h) instruction must be issued prior to a Write Status Register (01h) instruction. Write Enable for Volatile Status Register instruction (Figure 5) will not set the Write Enable Latch (WEL) bit, it is only valid for the Write Status Register instruction to change the volatile Status Register bit values.

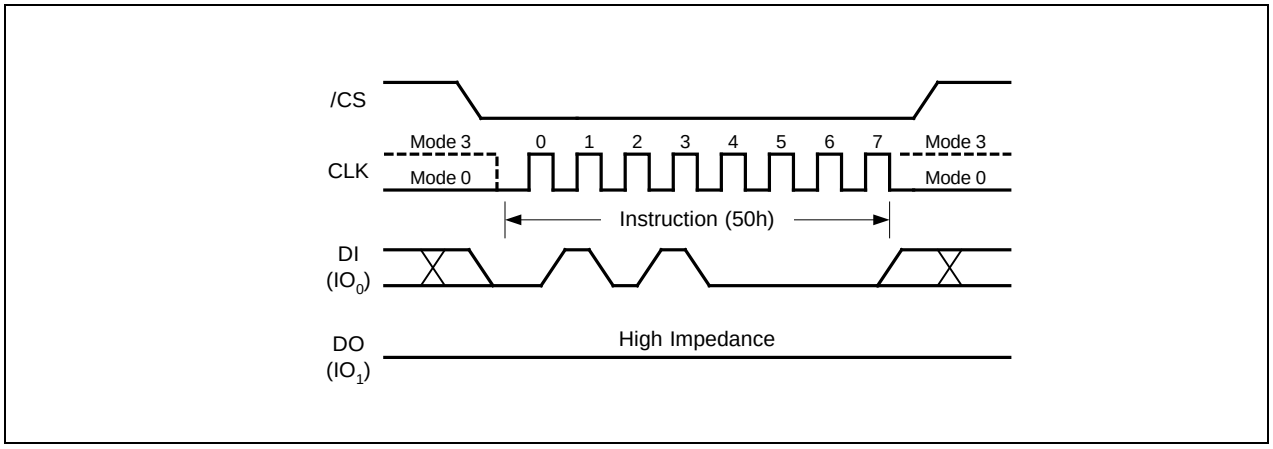


Figure 5. Write Enable for Volatile Status Register Instruction for SPI Mode

7.2.3 Write Disable (04h)

The Write Disable instruction (Figure 6) resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable instruction is entered by driving /CS low, shifting the instruction code “04h” into the DI pin and then driving /CS high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Erase/Program Security Registers, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase and Reset instructions.

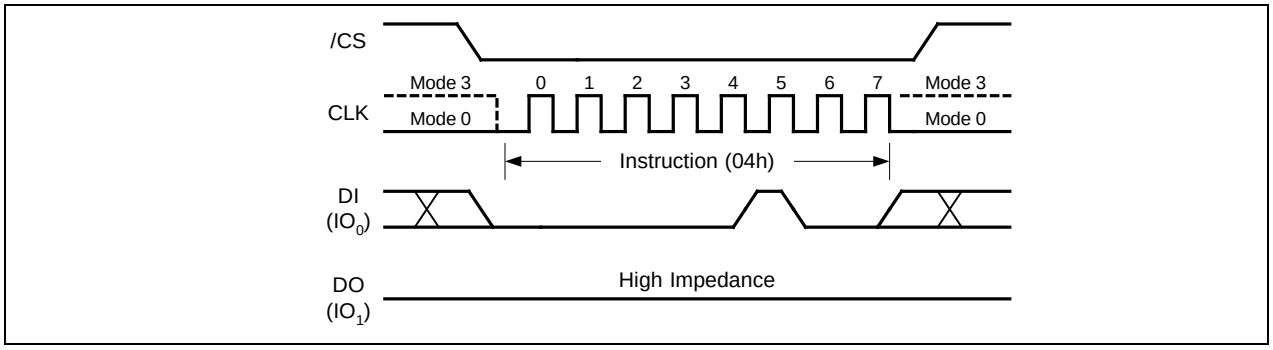


Figure 6. Write Disable Instruction for SPI Mode

7.2.4 Read Status Register-1 (05h), Status Register-2 (35h) & Status Register-3 (15h)

The Read Status Register instructions allow the 8-bit Status Registers to be read. The instruction is entered by driving /CS low and shifting the instruction code “05h” for Status Register-1, “35h” for Status Register-2 or “15h” for Status Register-3 into the DI pin on the rising edge of CLK. The status register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in Figure 7. Refer to section 6.1 for Status Register descriptions.

The Read Status Register instruction may be used at any time, even while a Program, Erase or Write Status Register cycle is in progress. This allows the BUSY status bit to be checked to determine when the cycle is complete and if the device can accept another instruction. The Status Register can be read continuously, as shown in Figure 7. The instruction is completed by driving /CS high.

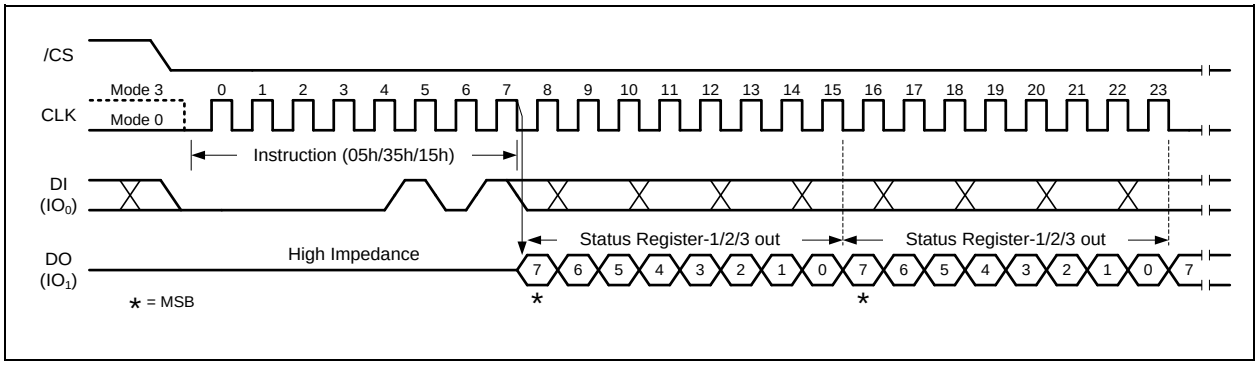


Figure 7. Read Status Register Instruction

7.2.5 Write Status Register-1 (01h), Status Register-2 (31h) & Status Register-3 (11h)

The Write Status Register instruction allows the Status Registers to be written. The writable Status Register bits include: SEC, TB, BP[2:0] in Status Register-1; CMP, LB[3:1], QE (only with part numbers ending in "IM"), SRL in Status Register-2; DRV1, DRV0, WPS in Status Register-3. QE bit of Status Register-2 is preset to 1, read-only status, and it cannot be cleared to 0 with part numbers ending in "IQ". All other Status Register bit locations are read-only and will not be affected by the Write Status Register instruction. LB[3:1] are non-volatile OTP bits, once it is set to 1, it cannot be cleared to 0.

To write non-volatile Status Register bits, a standard Write Enable (06h) instruction must previously have been executed for the device to accept the Write Status Register instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving /CS low, sending the instruction code "01h/31h/11h", and then writing the status register data byte as illustrated in Figure 8a.

To write volatile Status Register bits, a Write Enable for Volatile Status Register (50h) instruction must have been executed prior to the Write Status Register instruction (Status Register bit WEL remains 0). However, SRL and LB[3:1] cannot be changed from "1" to "0" because of the OTP protection for these bits. Upon power off or the execution of a Software/Hardware Reset, the volatile Status Register bit values will be lost, and the non-volatile Status Register bit values will be restored.

During non-volatile Status Register write operation (06h combined with 01h/31h/11h), after /CS is driven high, the self-timed Write Status Register cycle will commence for a time duration of tw (See AC Characteristics). While the Write Status Register cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Write Status Register cycle and a 0 when the cycle is finished and ready to accept other instructions again. After the Write Status Register cycle has finished, the Write Enable Latch (WEL) bit in the Status Register will be cleared to 0.

During volatile Status Register write operation (50h combined with 01h/31h/11h), after /CS is driven high, the Status Register bits will be refreshed to the new values within the time period of t_{SHSL2} (See AC Characteristics). BUSY bit will remain 0 during the Status Register bit refresh period.

Refer to section 6.1 for Status Register descriptions.

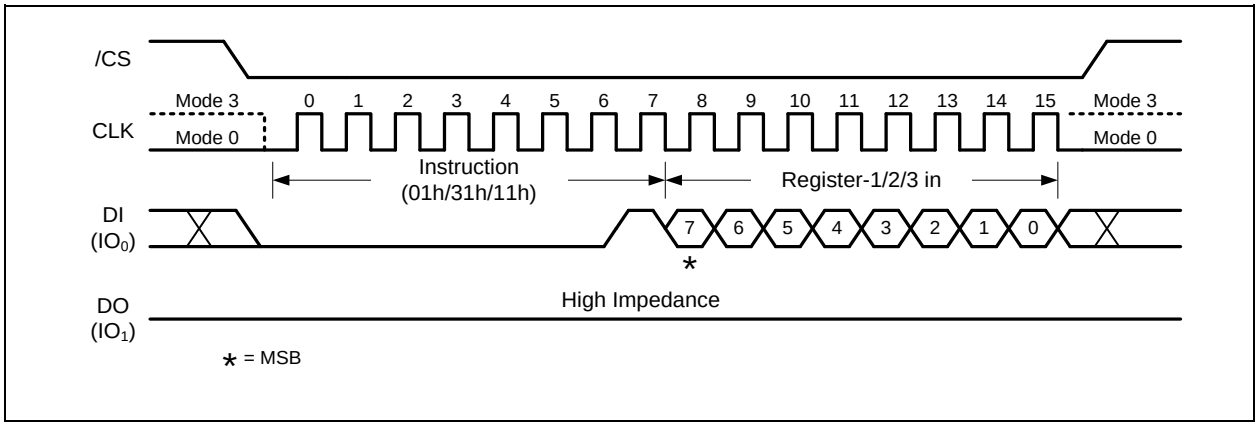


Figure 8a. Write Status Register-1/2/3 Instruction

The W25Q128JV is also backward compatible to Winbond's previous generations of serial flash memories, in which the Status Register-1&2 can be written using a single "Write Status Register-1 (01h)" command. To complete the Write Status Register-1&2 instruction, the /CS pin must be driven high after the sixteenth bit of data that is clocked in as shown in Figure 8b. If /CS is driven high after the eighth clock, the Write Status Register-1 (01h) instruction will only program the Status Register-1, the Status Register-2 will not be affected (Previous generations will clear CMP and QE bits). However, in part numbers ending with "IQ" configuration, QE bit of Status Register-2 is 'Read only', preset to '1', and will not be cleared to '0'.

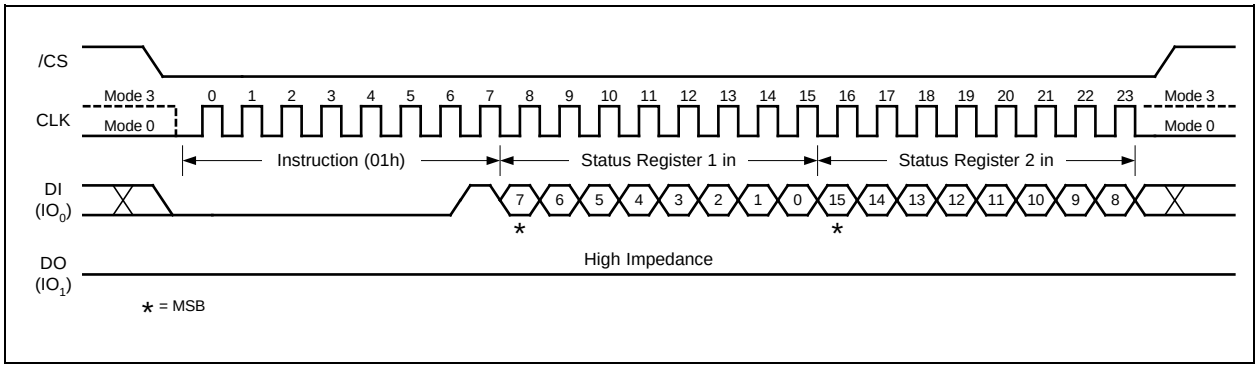


Figure 8b. Write Status Register-1/2 Instruction

7.2.6 Read Data (03h)

The Read Data instruction allows one or more data bytes to be sequentially read from the memory. The instruction is initiated by driving the /CS pin low and then shifting the instruction code “03h” followed by a 24-bit address (A23-A0) into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving /CS high.

The Read Data instruction sequence is shown in Figure 9. If a Read Data instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle. The Read Data instruction allows clock rates from D.C. to a maximum of f_R (see AC Electrical Characteristics).

The Read Data (03h) instruction is only supported in Standard SPI mode.

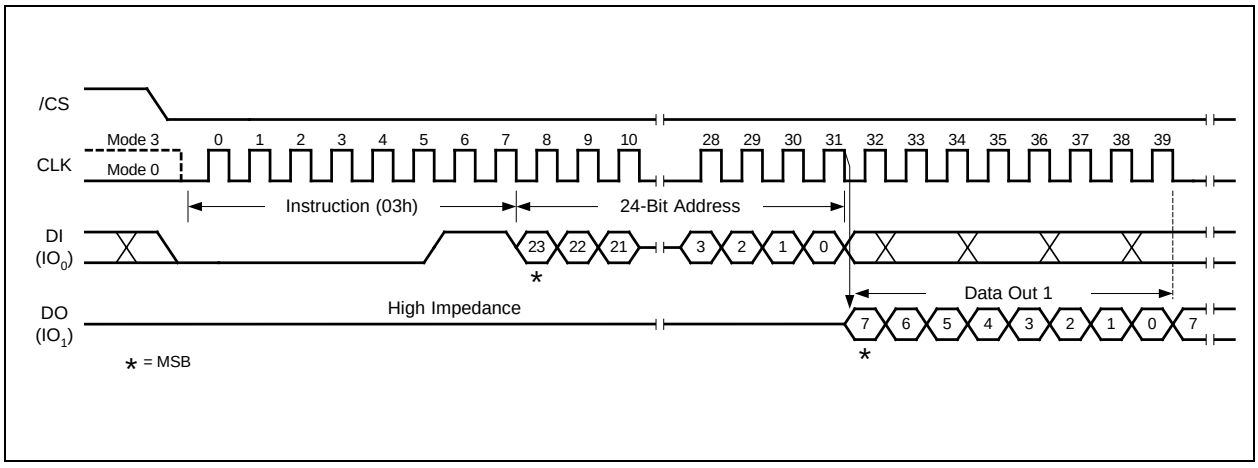


Figure 9. Read Data Instruction

7.2.7 Fast Read (0Bh)

The Fast Read instruction is similar to the Read Data instruction except that it can operate at the highest possible frequency of F_R (see AC Electrical Characteristics). This is accomplished by adding eight "dummy" clocks after the 24-bit address as shown in Figure 10. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the DO pin is a "don't care".

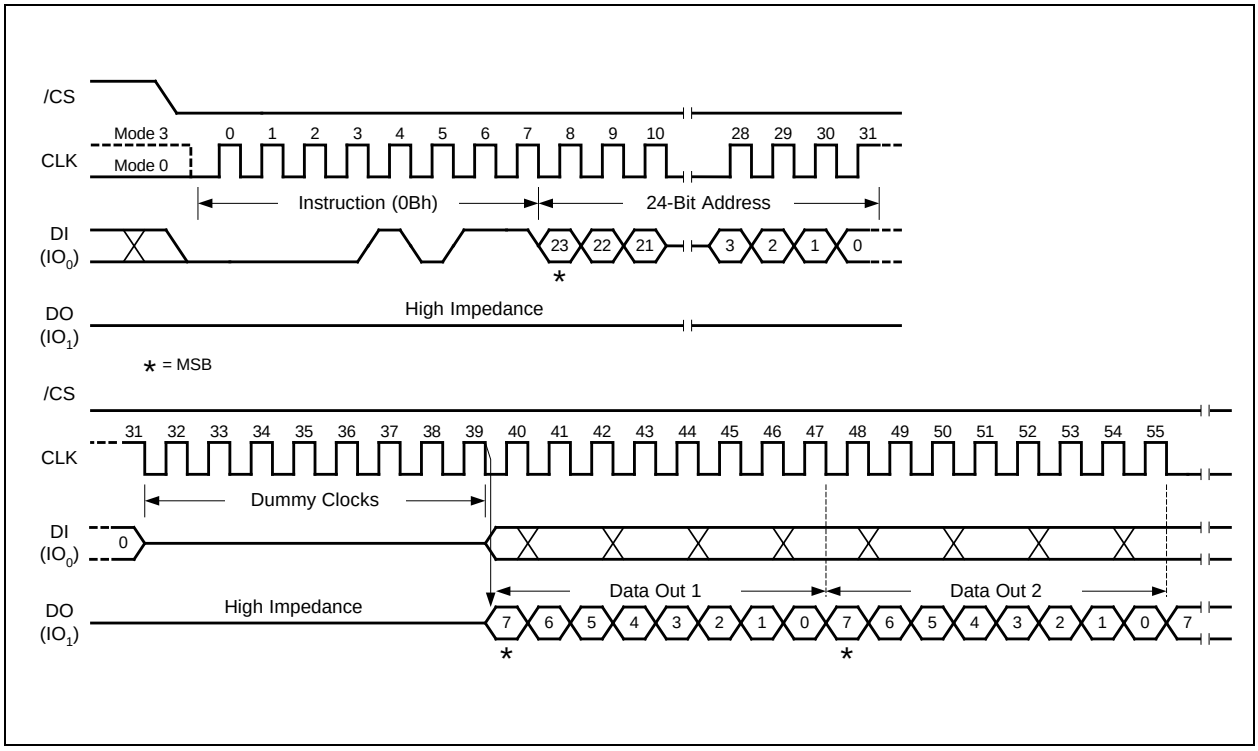


Figure 10. Fast Read Instruction

7.2.8 Fast Read Dual Output (3Bh)

The Fast Read Dual Output (3Bh) instruction is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins; IO_0 and IO_1. This allows data to be transferred at twice the rate of standard SPI devices. The Fast Read Dual Output instruction is ideal for quickly downloading code from Flash to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Similar to the Fast Read instruction, the Fast Read Dual Output instruction can operate at the highest possible frequency of F_R (see AC Electrical Characteristics). This is accomplished by adding eight "dummy" clocks after the 24-bit address as shown in Figure 11. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is "don't care". However, the IO_0 pin should be high-impedance prior to the falling edge of the first data out clock.

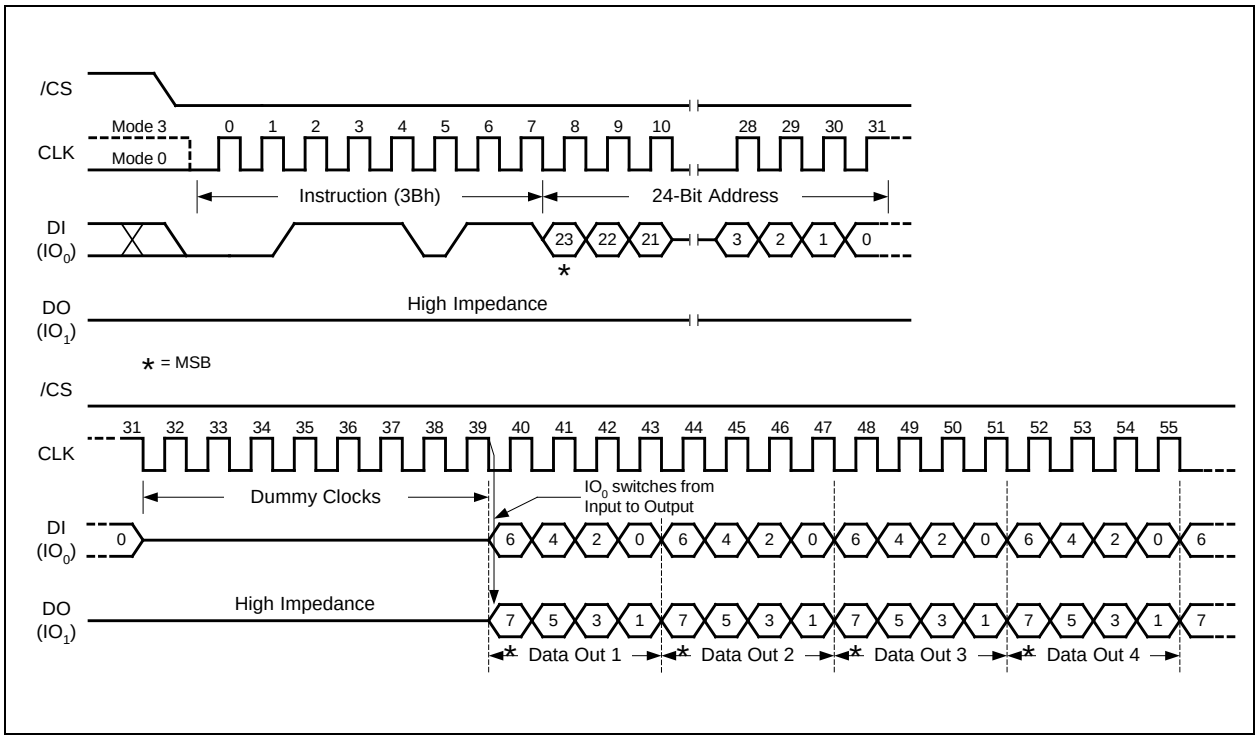


Figure 11. Fast Read Dual Output Instruction

7.2.9 Fast Read Quad Output (6Bh)

The Fast Read Quad Output (6Bh) instruction is similar to the Fast Read Dual Output (3Bh) instruction except that data is output on four pins, IO_0, IO_1, IO_2, and IO_3. The Quad Enable (QE) bit in Status Register-2 must be set to 1 before the device will accept the Fast Read Quad Output Instruction. The Fast Read Quad Output Instruction allows data to be transferred at four times the rate of standard SPI devices.

The Fast Read Quad Output instruction can operate at the highest possible frequency of F_R (see AC Electrical Characteristics). This is accomplished by adding eight "dummy" clocks after the 24-bit address as shown in Figure 12. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is "don't care". However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

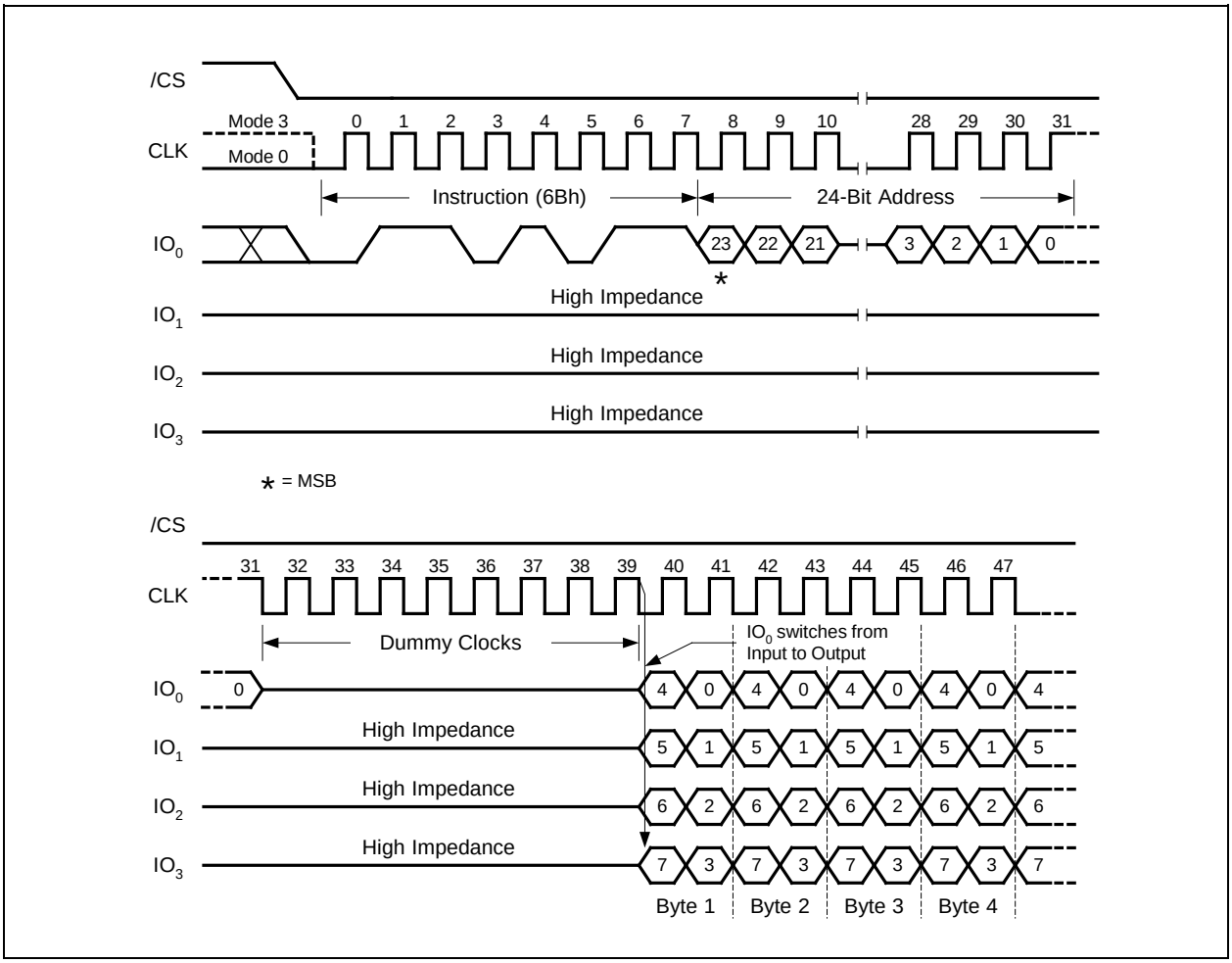


Figure 12. Fast Read Quad Output Instruction

7.2.10 Fast Read Dual I/O (BBh)

The Fast Read Dual I/O (BBh) instruction allows for improved random access while maintaining two IO pins, IO_0 and IO_1. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the Address bits (A23-0) two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

Similar to the Fast Read Dual Output (3Bh) instruction, the Fast Read Dual I/O instruction can operate at the highest possible frequency of F_R (see AC Electrical Characteristics). This is accomplished by adding four “dummy” clocks after the 24-bit address as shown in Figure 13. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care”. However, the IO_0 pin should be high-impedance prior to the falling edge of the first data out clock.

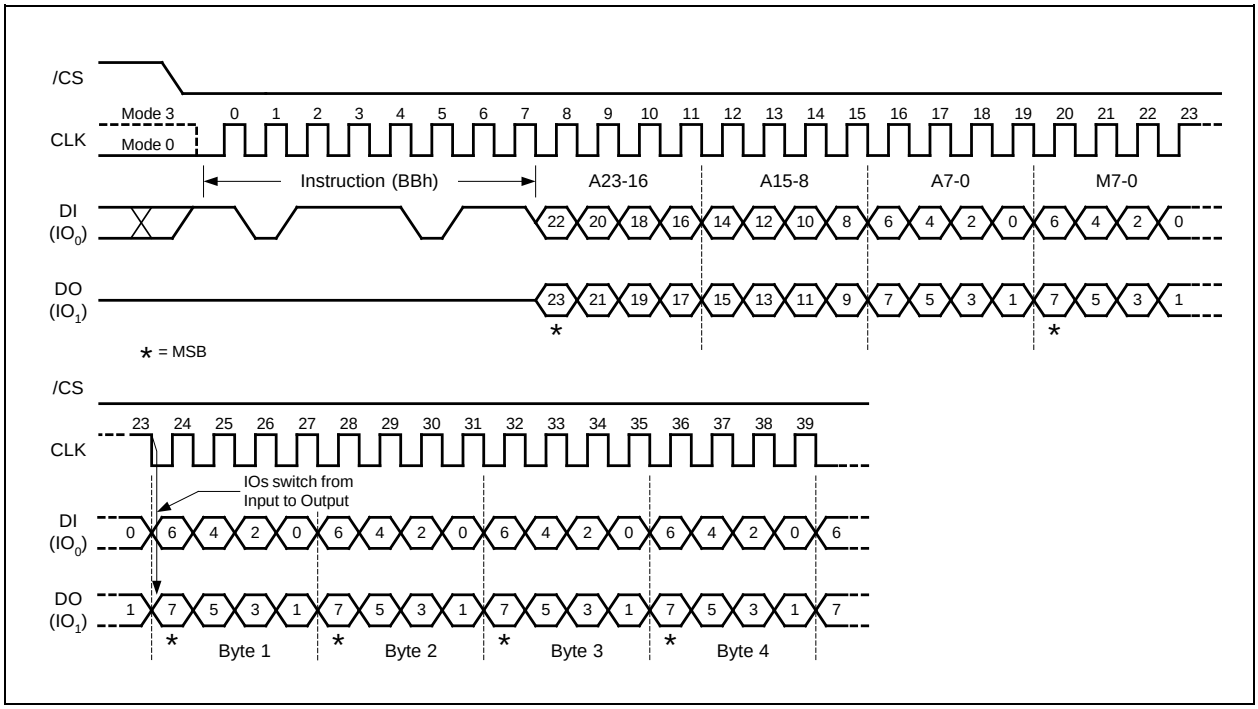


Figure 13. Fast Read Dual I/O Instruction (M7-M0 should be set to Fxh)

7.2.11 Fast Read Quad I/O (EBh)

The Fast Read Quad I/O (EBh) instruction is similar to the Fast Read Dual I/O (BBh) instruction except that address and data bits are input and output through four pins IO_0, IO_1, IO_2 and IO_3 and four Dummy clocks are required in SPI mode prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Fast Read Quad I/O Instruction.

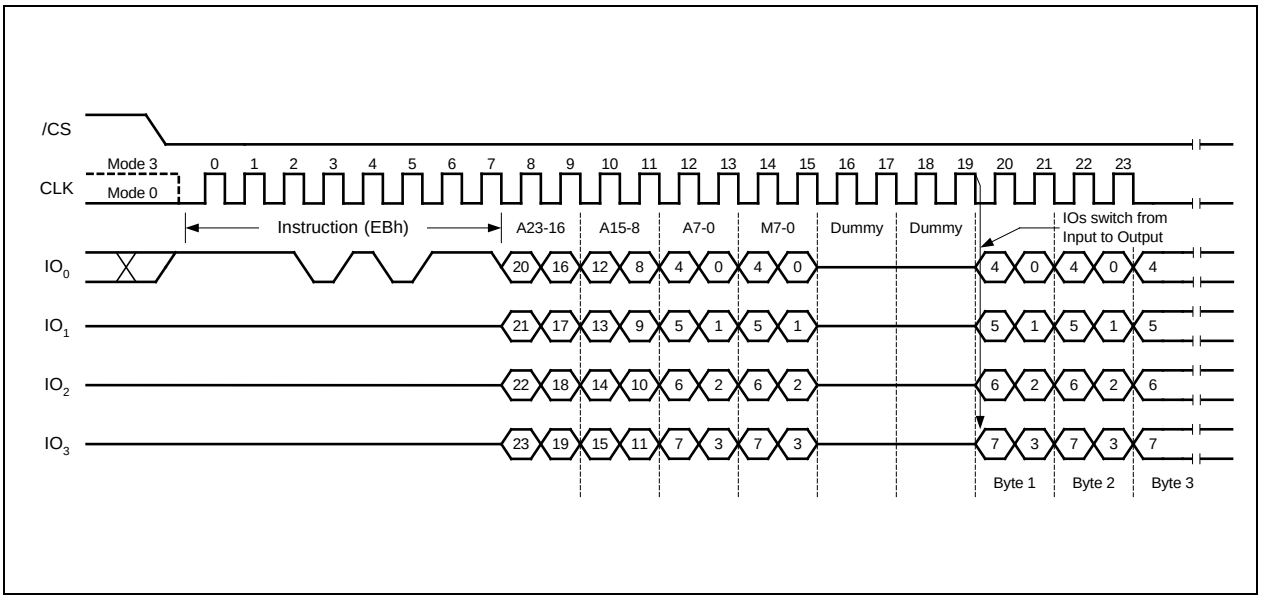


Figure 14. Fast Read Quad I/O Instruction (M7-M0 should be set to Fxh)

Fast Read Quad I/O with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

The Fast Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" (77h) command prior to EBh. The "Set Burst with Wrap" (77h) command can either enable or disable the "Wrap Around" feature for the following EBh commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

The "Set Burst with Wrap" instruction allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page. Refer to section 7.2.12 for detail descriptions.

7.2.12 Set Burst with Wrap (77h)

In Standard SPI mode, the Set Burst with Wrap (77h) instruction is used in conjunction with “Fast Read Quad I/O” instruction to access a fixed length of 8/16/32/64-byte section within a 256-byte page. Certain applications can benefit from this feature and improve the overall system code execution performance.

Similar to a Quad I/O instruction, the Set Burst with Wrap instruction is initiated by driving the /CS pin low and then shifting the instruction code “77h” followed by 24 dummy bits and 8 “Wrap Bits”, W7-0. The instruction sequence is shown in Figure 15. Wrap bit W7 and the lower nibble W3-0 are not used.

W6, W5	W4 = 0		W4 =1 (DEFAULT)	
	Wrap Around	Wrap Length	Wrap Around	Wrap Length
0 0	Yes	8-byte	No	N/A
0 1	Yes	16-byte	No	N/A
1 0	Yes	32-byte	No	N/A
1 1	Yes	64-byte	No	N/A

Once W6-4 is set by a Set Burst with Wrap instruction, all the following “Fast Read Quad I/O” instruction will use the W6-4 setting to access the 8/16/32/64-byte section within any page. To exit the “Wrap Around” function and return to normal read operation, another Set Burst with Wrap instruction should be issued to set W4 = 1. The default value of W4 upon power on or after a software/hardware reset is 1.

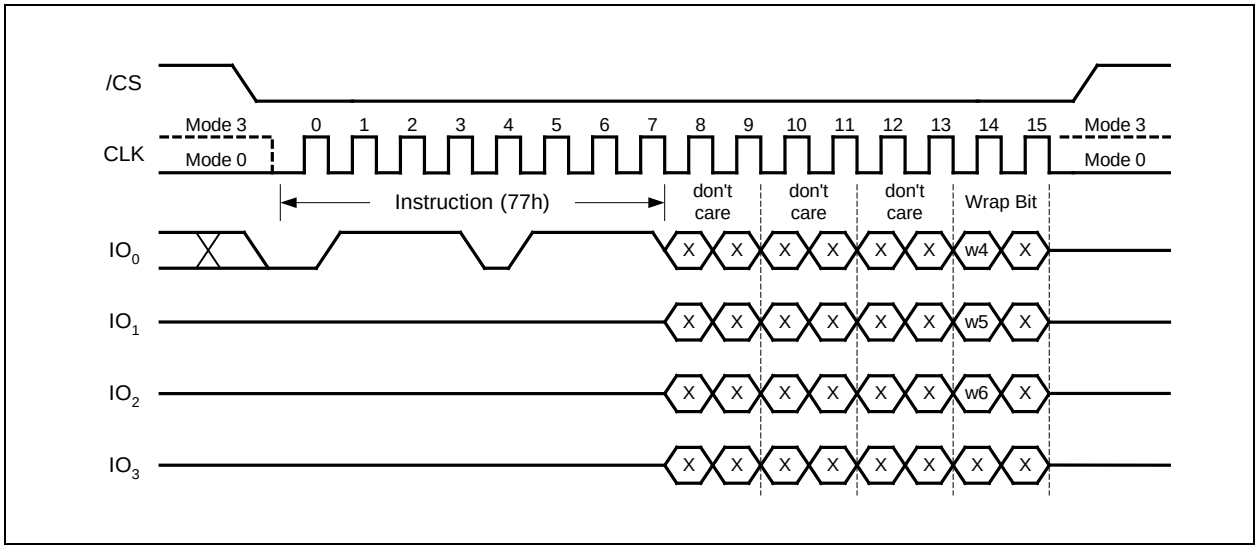


Figure 15. Set Burst with Wrap Instruction

7.2.13 Page Program (02h)

The Page Program instruction allows from one byte to 256 bytes (a page) of data to be programmed at previously erased (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Page Program Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the /CS pin low then shifting the instruction code “02h” followed by a 24-bit address (A23-A0) and at least one data byte, into the DI pin. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. The Page Program instruction sequence is shown in Figure 16.

If an entire 256 byte page is to be programmed, the last address byte (the 8 least significant address bits) should be set to 0. If the last address byte is not zero, and the number of clocks exceeds the remaining page length, the addressing will wrap to the beginning of the page. In some cases, less than 256 bytes (a partial page) can be programmed without having any effect on other bytes within the same page. One condition to perform a partial page program is that the number of clocks cannot exceed the remaining page length. If more than 256 bytes are sent to the device the addressing will wrap to the beginning of the page and overwrite previously sent data.

As with the write and erase instructions, the /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Page Program instruction will not be executed. After /CS is driven high, the self-timed Page Program instruction will commence for a time duration of tpp (See AC Characteristics). While the Page Program cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Page Program cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Page Program instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits or the Individual Block/Sector Locks.

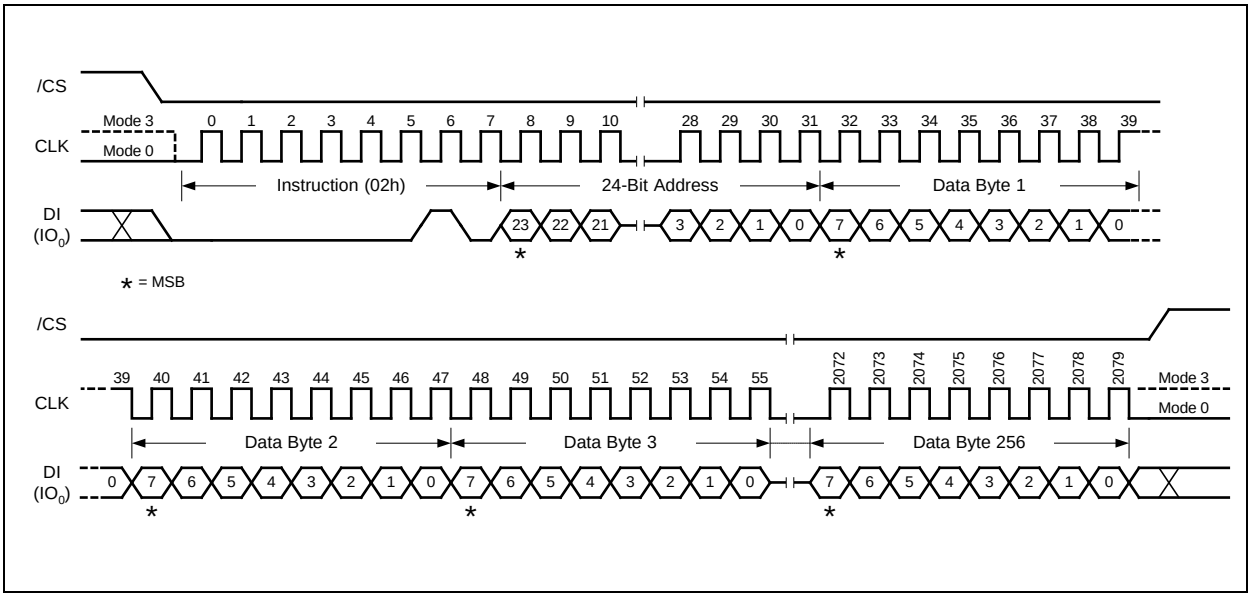


Figure 16. Page Program Instruction

7.2.14 Quad Input Page Program (32h)

The Quad Page Program instruction allows up to 256 bytes of data to be programmed at previously erased (FFh) memory locations using four pins: IO_0, IO_1, IO_2, and IO_3. The Quad Page Program can improve performance for PROM Programmer and applications that have slow clock speeds <5MHz. Systems with faster clock speed will not realize much benefit for the Quad Page Program instruction since the inherent page program time is much greater than the time it take to clock-in the data.

To use Quad Page Program the Quad Enable (QE) bit in Status Register-2 must be set to 1. A Write Enable instruction must be executed before the device will accept the Quad Page Program instruction (Status Register-1, WEL=1). The instruction is initiated by driving the /CS pin low then shifting the instruction code "32h" followed by a 24-bit address (A23-A0) and at least one data byte, into the IO pins. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. All other functions of Quad Page Program are identical to standard Page Program. The Quad Page Program instruction sequence is shown in Figure 17.

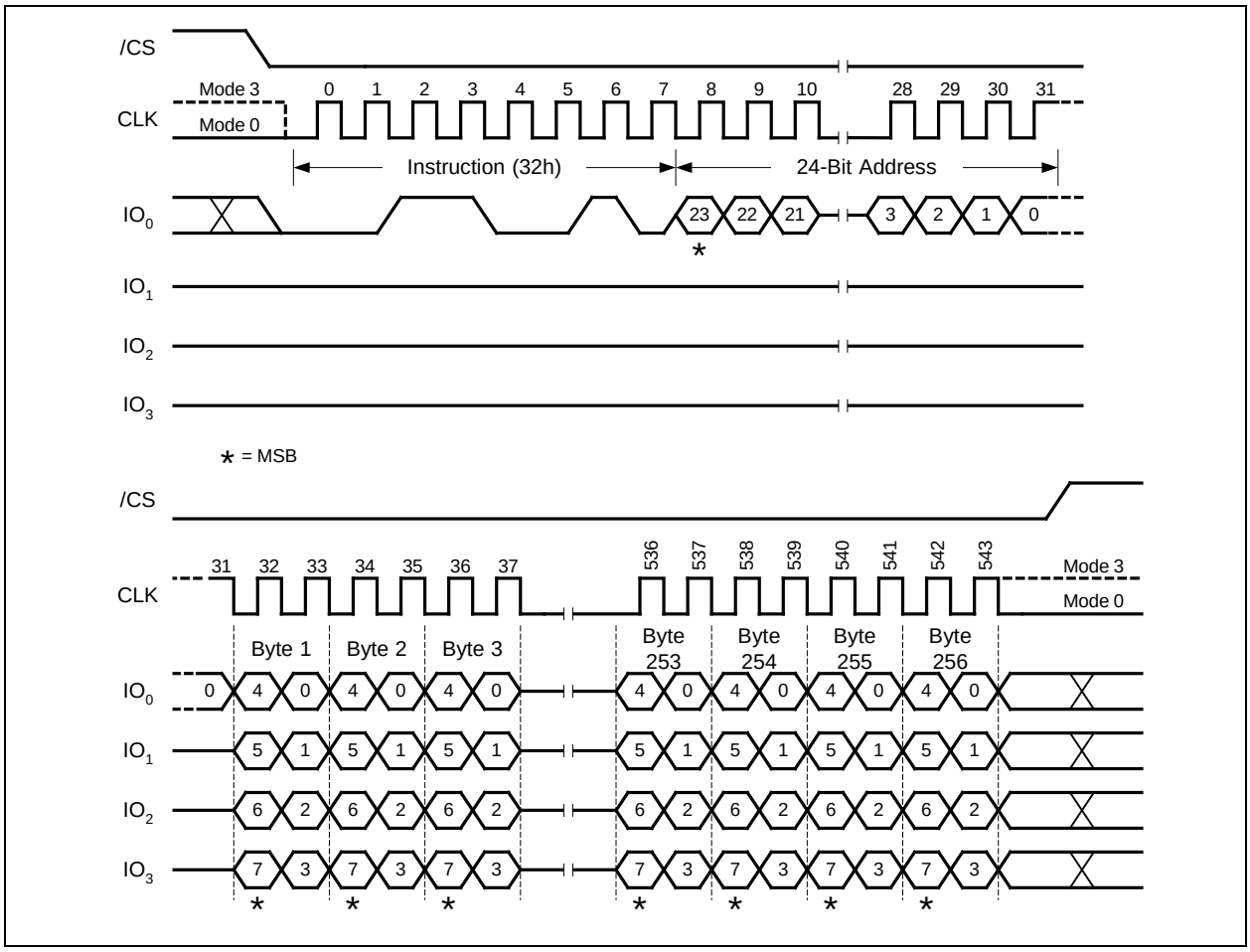


Figure 17. Quad Input Page Program Instruction

7.2.15 Sector Erase (20h)

The Sector Erase instruction sets all memory within a specified sector (4K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Sector Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “20h” followed a 24-bit sector address (A23-A0). The Sector Erase instruction sequence is shown in Figure 18.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Sector Erase instruction will not be executed. After /CS is driven high, the self-timed Sector Erase instruction will commence for a time duration of t_{SE} (See AC Characteristics). While the Sector Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Sector Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Sector Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Sector Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits or the Individual Block/Sector Locks.

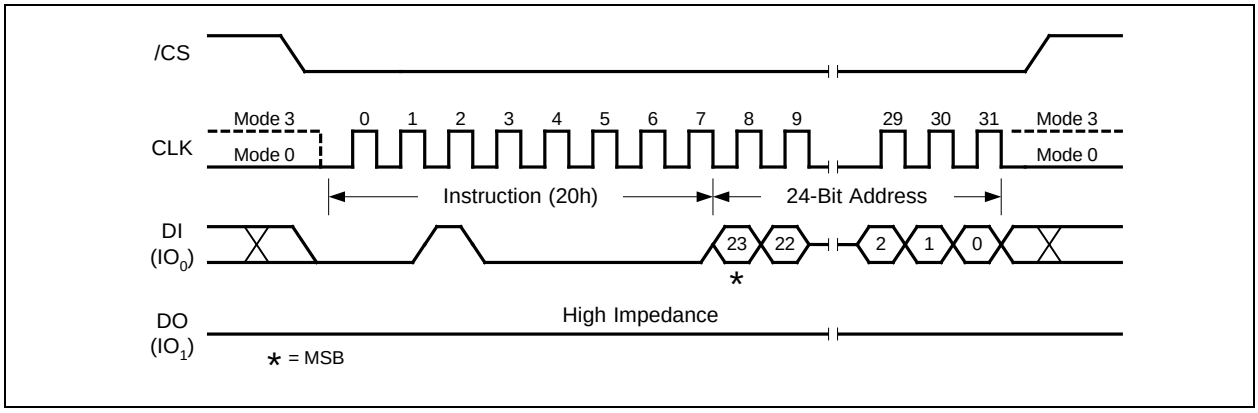


Figure 18. Sector Erase Instruction

7.2.16 32KB Block Erase (52h)

The Block Erase instruction sets all memory within a specified block (32K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code "52h" followed a 24-bit block address (A23-A0). The Block Erase instruction sequence is shown in Figure 19.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After /CS is driven high, the self-timed Block Erase instruction will commence for a time duration of t_{BE1} (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits or the Individual Block/Sector Locks.

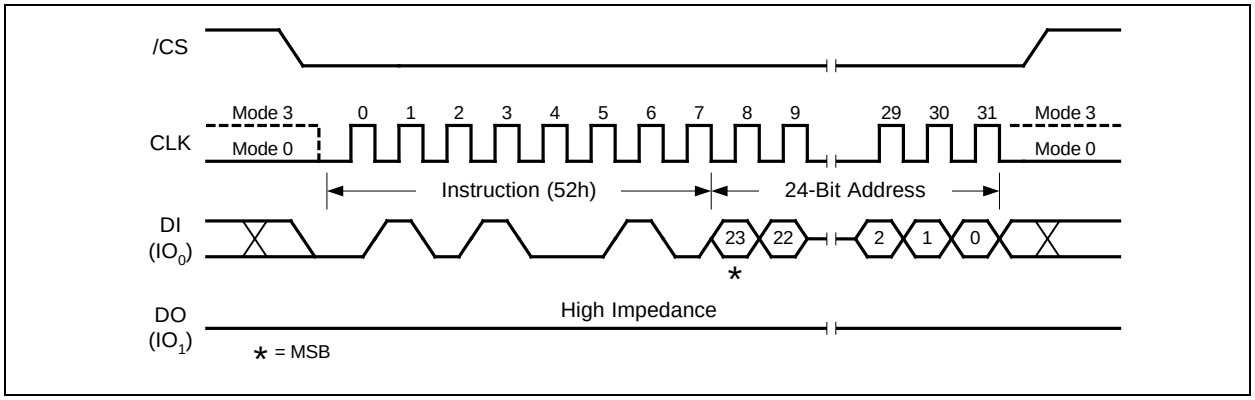


Figure 19. 32KB Block Erase Instruction

7.2.17 64KB Block Erase (D8h)

The Block Erase instruction sets all memory within a specified block (64K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code "D8h" followed a 24-bit block address (A23-A0). The Block Erase instruction sequence is shown in Figure 20.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After /CS is driven high, the self-timed Block Erase instruction will commence for a time duration of t_{BE} (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits or the Individual Block/Sector Locks.

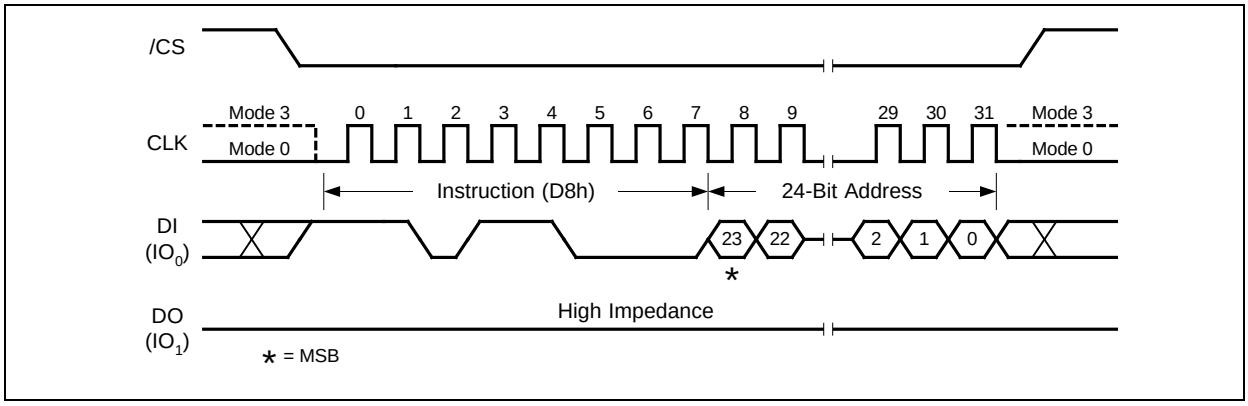


Figure 20. 64KB Block Erase Instruction

7.2.18 Chip Erase (C7h / 60h)

The Chip Erase instruction sets all memory within the device to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Chip Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “C7h” or “60h”. The Chip Erase instruction sequence is shown in Figure 21.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase instruction will not be executed. After /CS is driven high, the self-timed Chip Erase instruction will commence for a time duration of tCE (See AC Characteristics). While the Chip Erase cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other instructions again. After the Chip Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase instruction will not be executed if any memory region is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits or the Individual Block/Sector Locks.

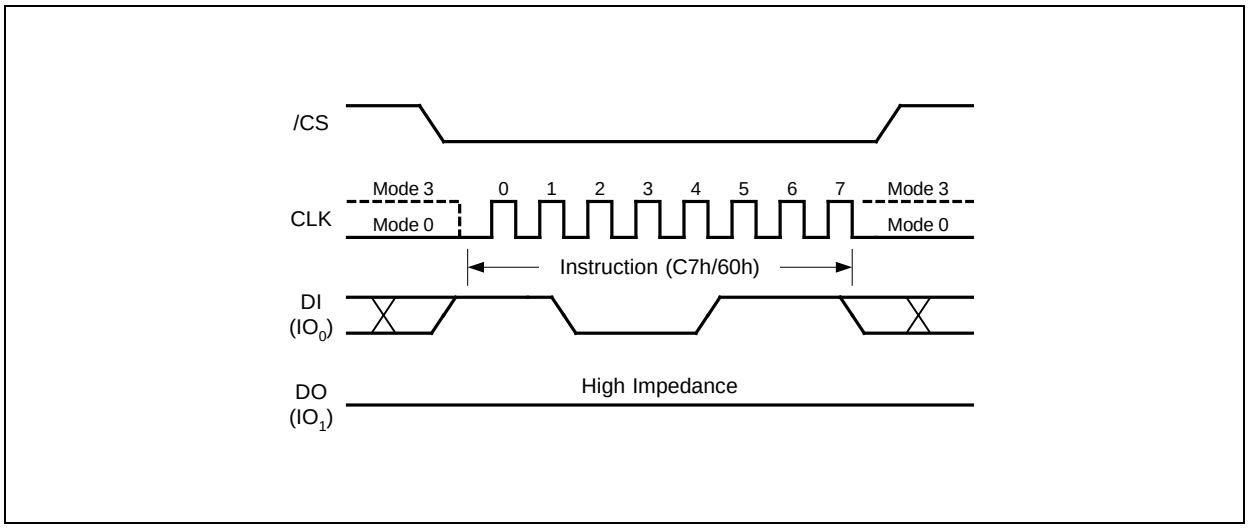


Figure 21. Chip Erase Instruction Sequence Diagram

7.2.19 Erase / Program Suspend (75h)

The Erase/Program Suspend instruction “75h”, allows the system to interrupt a Sector or Block Erase operation or a Page Program operation and then read from or program/erase data to, any other sectors or blocks. The Erase/Program Suspend instruction sequence is shown in Figure 22.

The Write Status Register instruction (01h) and Erase instructions (20h, 52h, D8h, C7h, 60h, 44h) are not allowed during Erase Suspend. Erase Suspend is valid only during the Sector or Block erase operation. If written during the Chip Erase operation, the Erase Suspend instruction is ignored. The Write Status Register instruction (01h) and Program instructions (02h, 32h, 42h) are not allowed during Program Suspend. Program Suspend is valid only during the Page Program or Quad Page Program operation.

The Erase/Program Suspend instruction “75h” will be accepted by the device only if the SUS bit in the Status Register equals to 0 and the BUSY bit equals to 1 while a Sector or Block Erase or a Page Program operation is on-going. If the SUS bit equals to 1 or the BUSY bit equals to 0, the Suspend instruction will be ignored by the device. A maximum of time of “t_{SUS}” (See AC Characteristics) is required to suspend the erase or program operation. The BUSY bit in the Status Register will be cleared from 1 to 0 within “t_{SUS}” and the SUS bit in the Status Register will be set from 0 to 1 immediately after Erase/Program Suspend. For a previously resumed Erase/Program operation, it is also required that the Suspend instruction “75h” is not issued earlier than a minimum of time of “t_{SUS}” following the preceding Resume instruction “7Ah”.

Unexpected power off during the Erase/Program suspend state will reset the device and release the suspend state. SUS bit in the Status Register will also reset to 0. The data within the page, sector or block that was being suspended may become corrupted. It is recommended for the user to implement system design techniques against the accidental power interruption and preserve data integrity during erase/program suspend state.

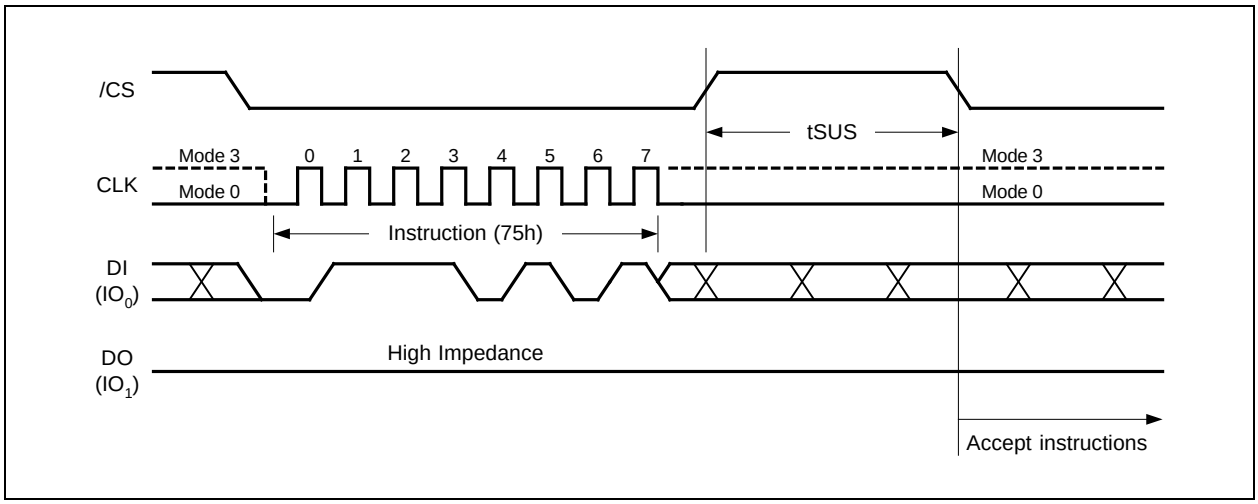


Figure 22. Erase/Program Suspend Instruction

7.2.20 Erase / Program Resume (7Ah)

The Erase/Program Resume instruction “7Ah” must be written to resume the Sector or Block Erase operation or the Page Program operation after an Erase/Program Suspend. The Resume instruction “7Ah” will be accepted by the device only if the SUS bit in the Status Register equals to 1 and the BUSY bit equals to 0. After issued the SUS bit will be cleared from 1 to 0 immediately, the BUSY bit will be set from 0 to 1 within 200ns and the Sector or Block will complete the erase operation or the page will complete the program operation. If the SUS bit equals to 0 or the BUSY bit equals to 1, the Resume instruction “7Ah” will be ignored by the device. The Erase/Program Resume instruction sequence is shown in Figure 23.

Resume instruction is ignored if the previous Erase/Program Suspend operation was interrupted by unexpected power off. It is also required that a subsequent Erase/Program Suspend instruction not to be issued within a minimum of time of “t_{SUS}” following a previous Resume instruction.

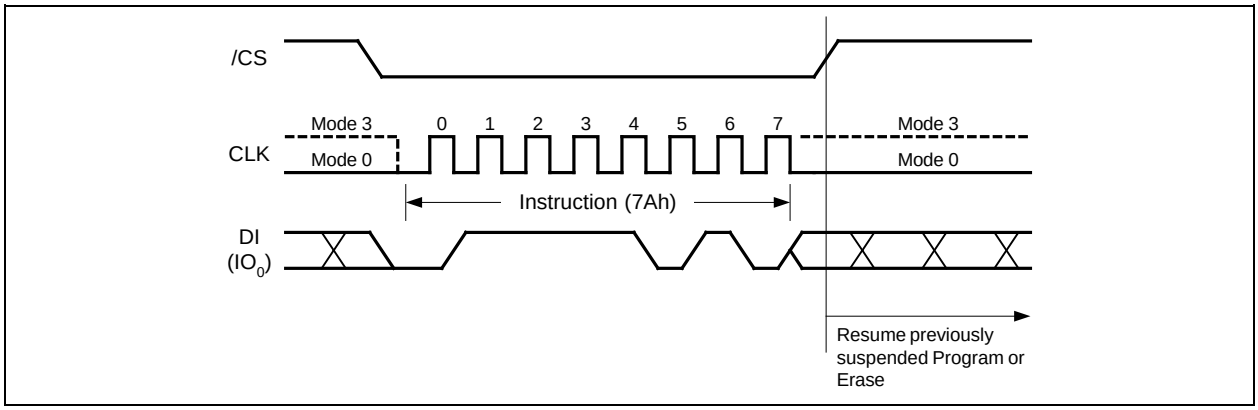


Figure 23. Erase/Program Resume Instruction

7.2.21 Power-down (B9h)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Power-down instruction. The lower power consumption makes the Power-down instruction especially useful for battery powered applications (See ICC1 and ICC2 in AC Characteristics). The instruction is initiated by driving the /CS pin low and shifting the instruction code “B9h” as shown in Figure 24.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Power-down instruction will not be executed. After /CS is driven high, the power-down state will entered within the time duration of t_{DP} (See AC Characteristics). While in the power-down state only the Release Power-down / Device ID (ABh) instruction, which restores the device to normal operation, will be recognized. All other instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring all but one instruction makes the Power Down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of ICC1.

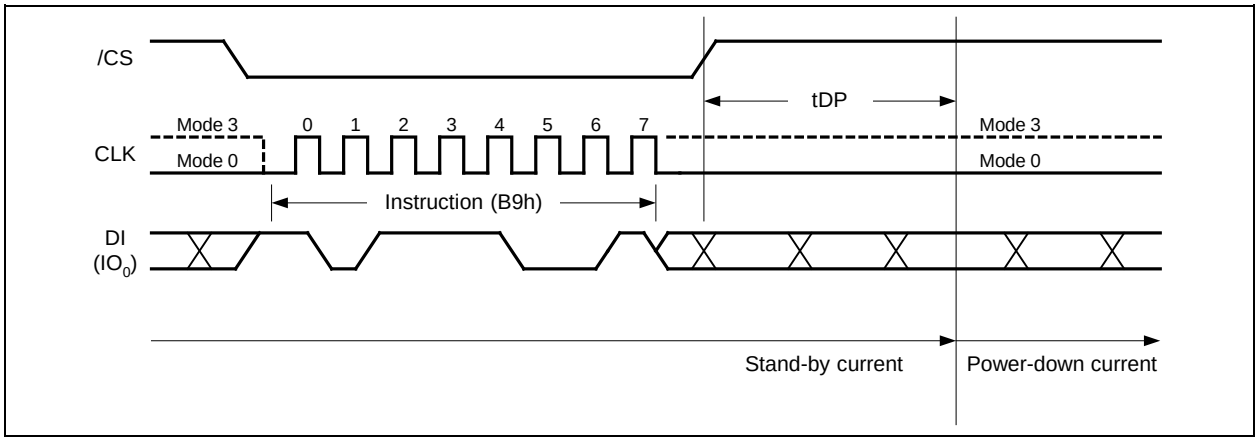


Figure 24. Deep Power-down Instruction

7.2.22 Release Power-down / Device ID (ABh)

The Release from Power-down / Device ID instruction is a multi-purpose instruction. It can be used to release the device from the power-down state, or obtain the devices electronic identification (ID) number.

To release the device from the power-down state, the instruction is issued by driving the /CS pin low, shifting the instruction code "ABh" and driving /CS high as shown in Figure 25a. Release from power-down will take the time duration of t_{RES1} (See AC Characteristics) before the device will resume normal operation and other instructions are accepted. The /CS pin must remain high during the t_{RES1} time duration.

When used only to obtain the Device ID while not in the power-down state, the instruction is initiated by driving the /CS pin low and shifting the instruction code "ABh" followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of CLK with most significant bit (MSB) first. The Device ID value for the W25Q128JV is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The instruction is completed by driving /CS high.

When used to release the device from the power-down state and obtain the Device ID, the instruction is the same as previously described, and shown in Figure 25b, except that after /CS is driven high it must remain high for a time duration of t_{RES2} (See AC Characteristics). After this time duration the device will resume normal operation and other instructions will be accepted. If the Release from Power-down / Device ID instruction is issued while an Erase, Program or Write cycle is in process (when BUSY equals 1) the instruction is ignored and will not have any effects on the current cycle.

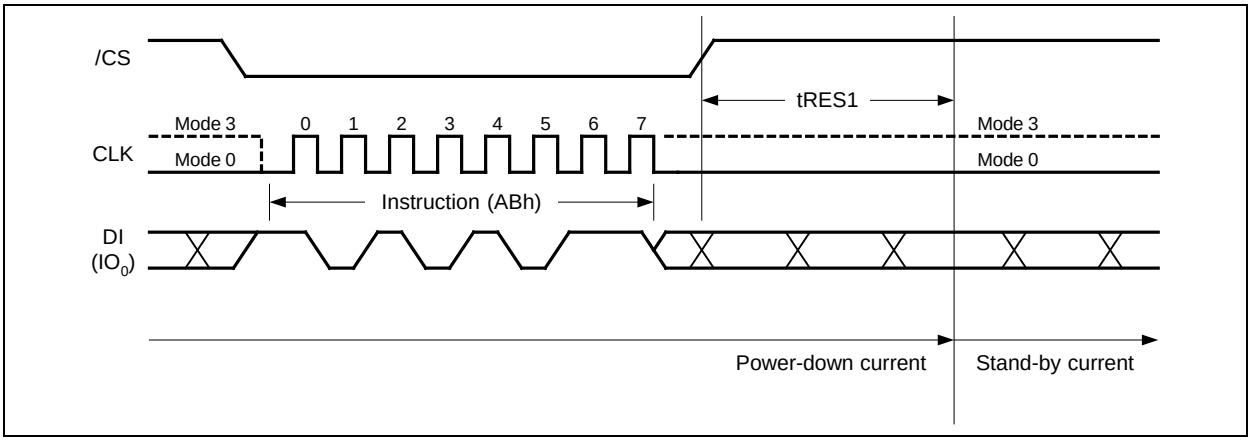


Figure 25a. Release Power-down Instruction

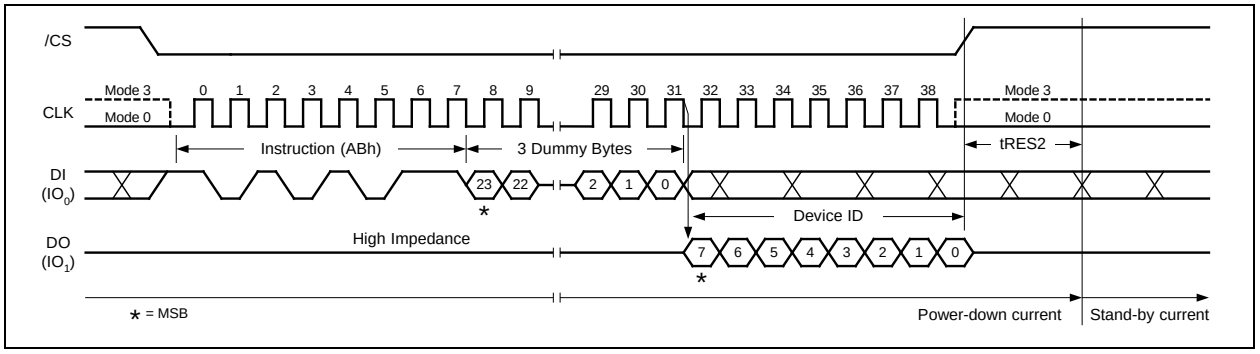


Figure 25b. Release Power-down / Device ID Instruction

7.2.23 Read Manufacturer / Device ID (90h)

The Read Manufacturer/Device ID instruction is an alternative to the Release from Power-down / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/Device ID instruction is very similar to the Release from Power-down / Device ID instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code "90h" followed by a 24-bit address (A23-A0) of 000000h. After which, the Manufacturer ID for Winbond (EFh) and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 26. The Device ID values for the W25Q128JV are listed in Manufacturer and Device Identification table. The instruction is completed by driving /CS high.

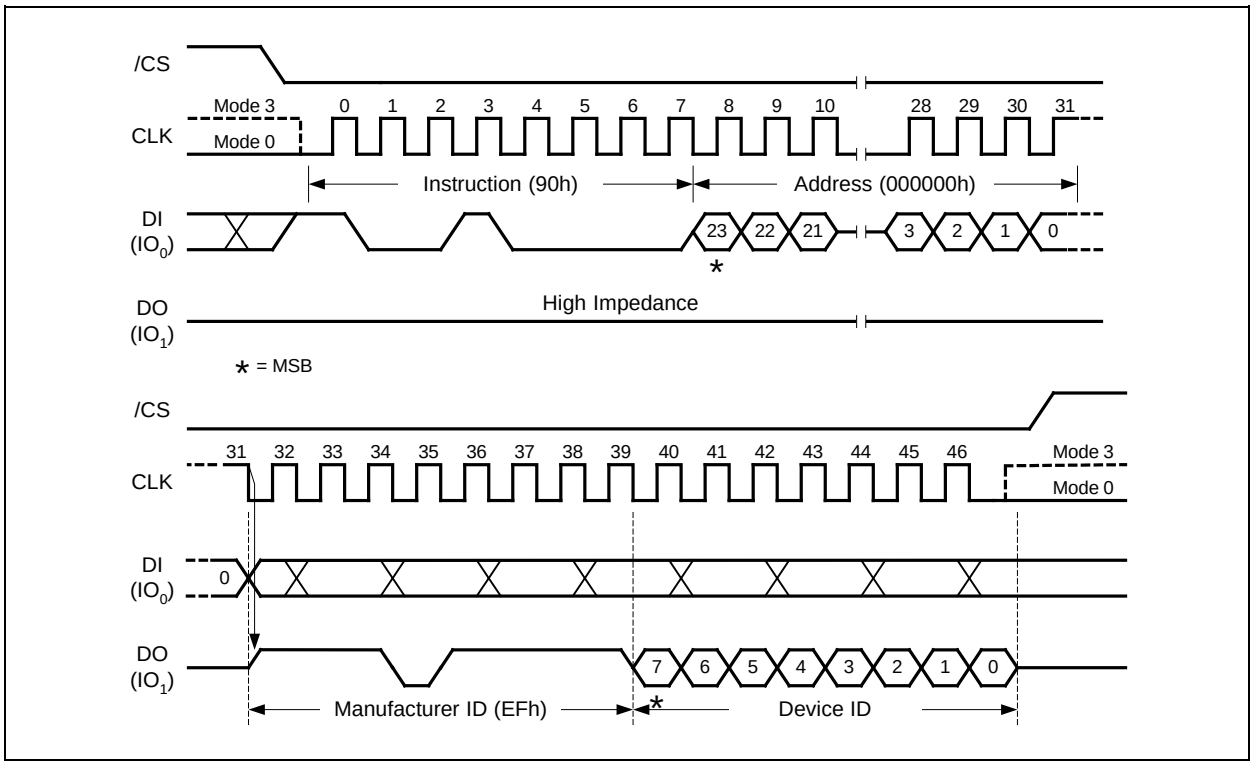


Figure 26. Read Manufacturer / Device ID Instruction

7.2.24 Read Manufacturer / Device ID Dual I/O (92h)

The Read Manufacturer / Device ID Dual I/O instruction is an alternative to the Read Manufacturer / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID at 2x speed.

The Read Manufacturer / Device ID Dual I/O instruction is similar to the Fast Read Dual I/O instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code "92h" followed by a 24-bit address (A23-A0) of 000000h, but with the capability to input the Address bits two bits per clock. After which, the Manufacturer ID for Winbond (EFh) and the Device ID are shifted out 2 bits per clock on the falling edge of CLK with most significant bits (MSB) first as shown in Figure 27. The Device ID values for the W25Q128JV are listed in Manufacturer and Device Identification table. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving /CS high.

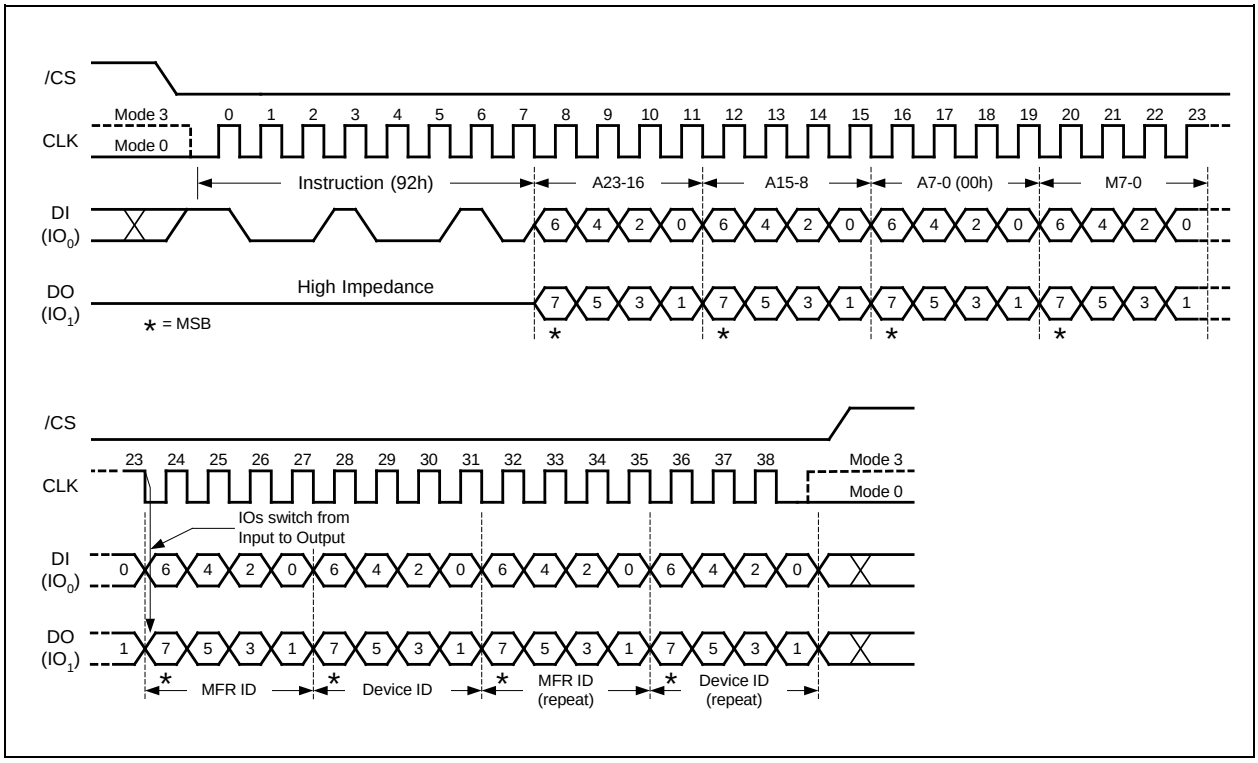


Figure 27. Read Manufacturer / Device ID Dual I/O Instruction

Note:

The "Continuous Read Mode" bits M(7-0) must be set to Fxh to be compatible with Fast Read Dual I/O instruction.

7.2.25 Read Manufacturer / Device ID Quad I/O (94h)

The Read Manufacturer / Device ID Quad I/O instruction is an alternative to the Read Manufacturer / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID at 4x speed.

The Read Manufacturer / Device ID Quad I/O instruction is similar to the Fast Read Quad I/O instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code "94h" followed by a four clock dummy cycles and then a 24-bit address (A23-A0) of 000000h, but with the capability to input the Address bits four bits per clock. After which, the Manufacturer ID for Winbond (EFh) and the Device ID are shifted out four bits per clock on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 28. The Device ID values for the W25Q128JV are listed in Manufacturer and Device Identification table. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving /CS high.

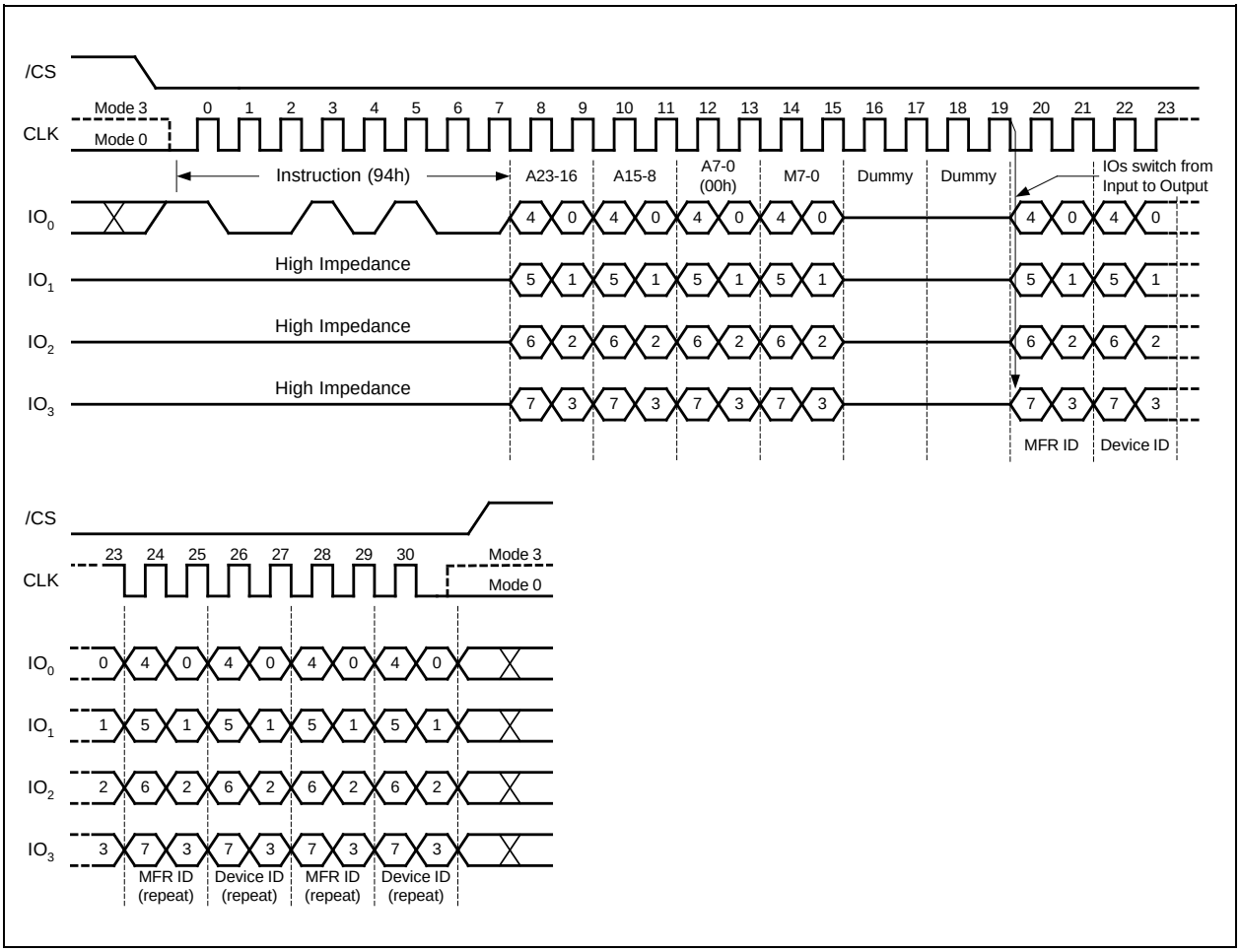


Figure 28. Read Manufacturer / Device ID Quad I/O Instruction

Note:

The "Continuous Read Mode" bits M(7-0) must be set to Fxh to be compatible with Fast Read Quad I/O instruction.

7.2.26 Read Unique ID Number (4Bh)

The Read Unique ID Number instruction accesses a factory-set read-only 64-bit number that is unique to each W25Q128JV device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID instruction is initiated by driving the /CS pin low and shifting the instruction code “4Bh” followed by a four bytes of dummy clocks. After which, the 64-bit ID is shifted out on the falling edge of CLK as shown in Figure 29.

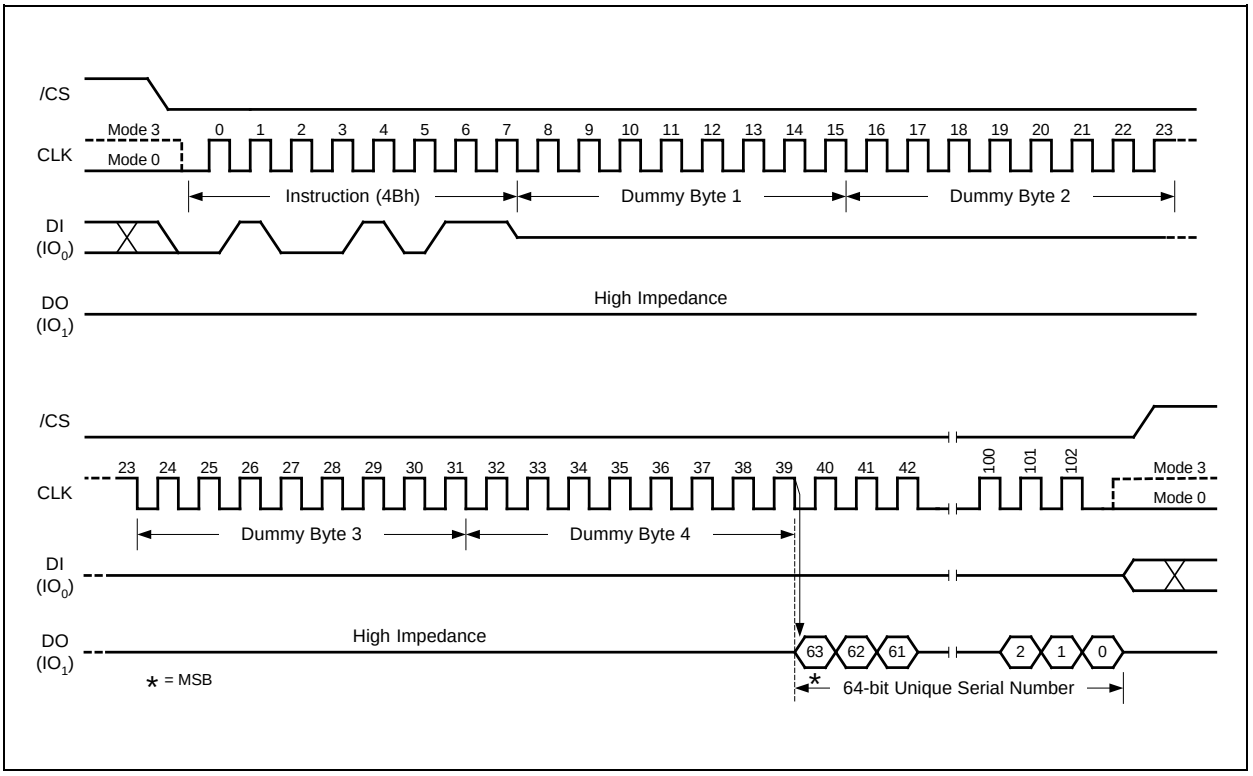


Figure 29. Read Unique ID Number Instruction

7.2.27 Read JEDEC ID (9Fh)

For compatibility reasons, the W25Q128JV provides several instructions to electronically determine the identity of the device. The Read JEDEC ID instruction is compatible with the JEDEC standard for SPI compatible serial memories that was adopted in 2003. The instruction is initiated by driving the /CS pin low and shifting the instruction code “9Fh”. The JEDEC assigned Manufacturer ID byte for Winbond (EFh) and two Device ID bytes, Memory Type (ID15-ID8) and Capacity (ID7-ID0) are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 30. For memory type and capacity values refer to Manufacturer and Device Identification table.

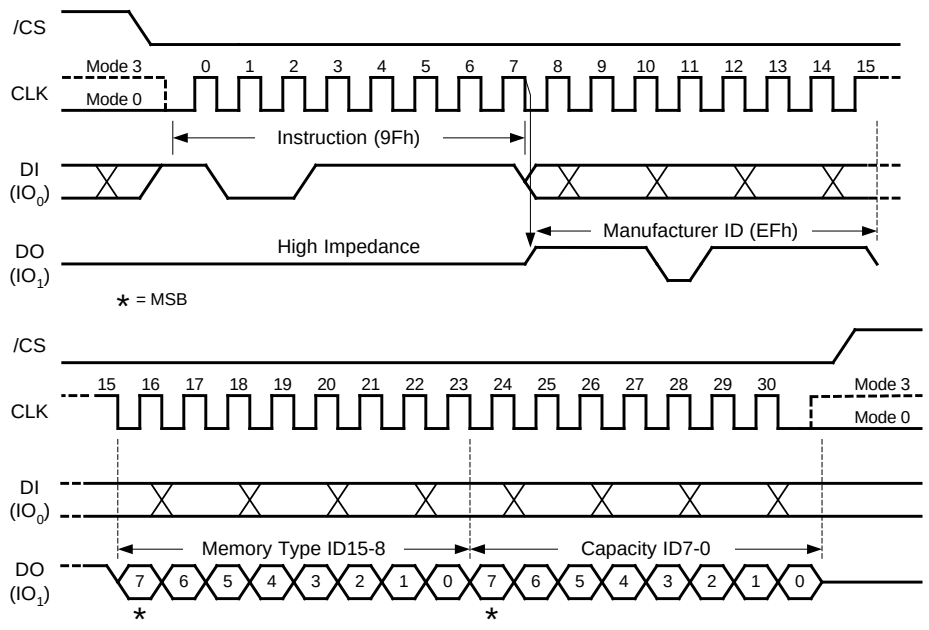


Figure 30. Read JEDEC ID Instruction

7.2.28 Read SFDP Register (5Ah)

The W25Q128JV features a 256-Byte Serial Flash Discoverable Parameter (SFDP) register that contains information about device configurations, available instructions and other features. The SFDP parameters are stored in one or more Parameter Identification (PID) tables. Currently only one PID table is specified, but more may be added in the future. The Read SFDP Register instruction is compatible with the SFDP standard initially established in 2010 for PC and other applications, as well as the JEDEC standard JESD216-serials that is published in 2011. Most Winbond SpiFlash Memories shipped after June 2011 (date code 1124 and beyond) support the SFDP feature as specified in the applicable datasheet.

The Read SFDP instruction is initiated by driving the /CS pin low and shifting the instruction code "5Ah" followed by a 24-bit address (A23-A0)(1) into the DI pin. Eight "dummy" clocks are also required before the SFDP register contents are shifted out on the falling edge of the 40th CLK with most significant bit (MSB) first as shown in Figure 31. For SFDP register values and descriptions, please refer to the Winbond Application Note for SFDP Definition Table.

Note 1: A23-A8 = 0; A7-A0 are used to define the starting byte address for the 256-Byte SFDP Register.

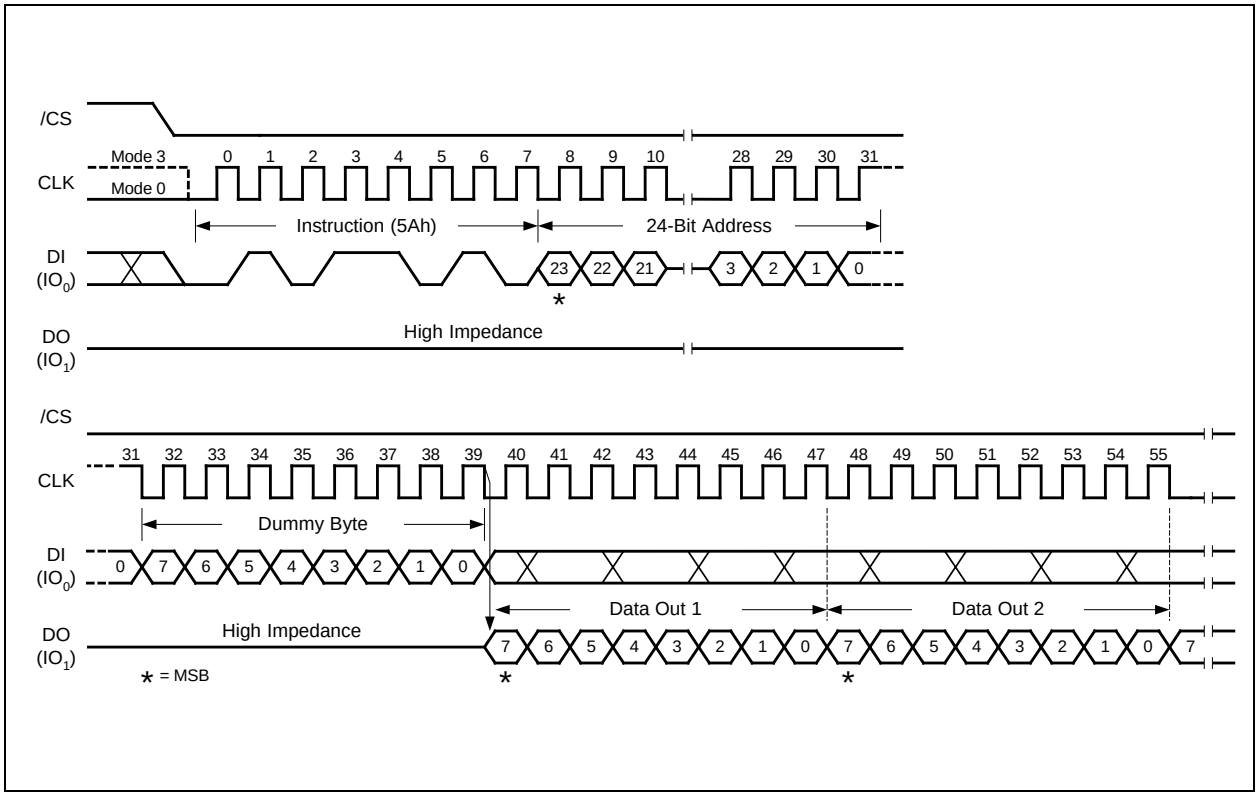


Figure 31. Read SFDP Register Instruction Sequence Diagram

7.2.29 Erase Security Registers (44h)

The W25Q128JV offers three 256-byte Security Registers which can be erased and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Register instruction is similar to the Sector Erase instruction. A Write Enable instruction must be executed before the device will accept the Erase Security Register Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “44h” followed by a 24-bit address (A23-A0) to erase one of the three security registers.

ADDRESS	A23-16	A15-12	A11-8	A7-0
Security Register #1	00h	0 0 0 1	0 0 0 0	Don’t Care
Security Register #2	00h	0 0 1 0	0 0 0 0	Don’t Care
Security Register #3	00h	0 0 1 1	0 0 0 0	Don’t Care

The Erase Security Register instruction sequence is shown in Figure 32. The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the instruction will not be executed. After /CS is driven high, the self-timed Erase Security Register operation will commence for a time duration of t_{SE} (See AC Characteristics). While the Erase Security Register cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Erase Security Register cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Security Register Lock Bits (LB3-1) in the Status Register-2 can be used to OTP protect the security registers. Once a lock bit is set to 1, the corresponding security register will be permanently locked, Erase Security Register instruction to that register will be ignored (Refer to section 6.1.9 for detail descriptions).

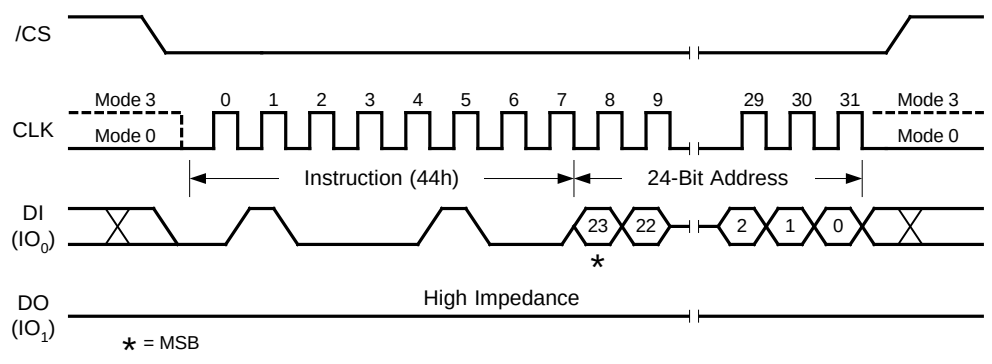


Figure 32. Erase Security Registers Instruction

7.2.30 Program Security Registers (42h)

The Program Security Register instruction is similar to the Page Program instruction. It allows from one byte to 256 bytes of security register data to be programmed at previously erased (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Program Security Register Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the /CS pin low then shifting the instruction code “42h” followed by a 24-bit address (A23-A0) and at least one data byte, into the DI pin. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device.

ADDRESS	A23-16	A15-12	A11-8	A7-0
Security Register #1	00h	0 0 0 1	0 0 0 0	Byte Address
Security Register #2	00h	0 0 1 0	0 0 0 0	Byte Address
Security Register #3	00h	0 0 1 1	0 0 0 0	Byte Address

The Program Security Register instruction sequence is shown in Figure 33. The Security Register Lock Bits (LB3-1) in the Status Register-2 can be used to OTP protect the security registers. Once a lock bit is set to 1, the corresponding security register will be permanently locked, Program Security Register instruction to that register will be ignored (See 6.1.9 for detail descriptions).

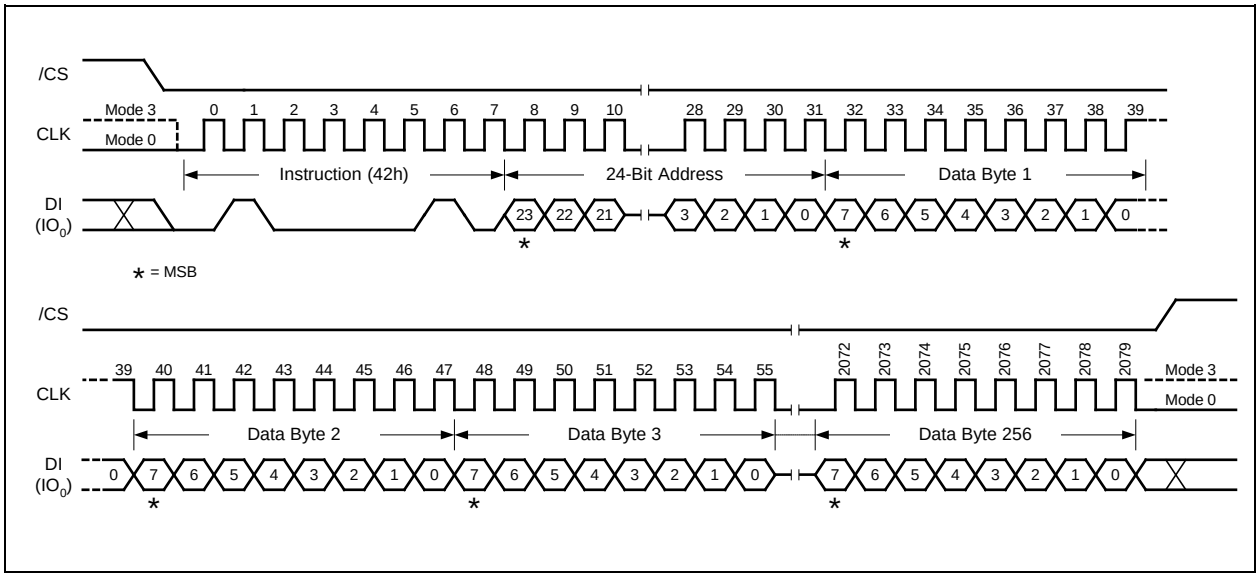


Figure 33. Program Security Registers Instruction

7.2.31 Read Security Registers (48h)

The Read Security Register instruction is similar to the Fast Read instruction and allows one or more data bytes to be sequentially read from one of the four security registers. The instruction is initiated by driving the /CS pin low and then shifting the instruction code “48h” followed by a 24-bit address (A23-A0) and eight “dummy” clocks into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The byte address is automatically incremented to the next byte address after each byte of data is shifted out. Once the byte address reaches the last byte of the register (byte address FFh), it will reset to address 00h, the first byte of the register, and continue to increment. The instruction is completed by driving /CS high. The Read Security Register instruction sequence is shown in Figure 34. If a Read Security Register instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle. The Read Security Register instruction allows clock rates from D.C. to a maximum of FR (see AC Electrical Characteristics).

ADDRESS	A23-16	A15-12	A11-8	A7-0
Security Register #1	00h	0 0 0 1	0 0 0 0	Byte Address
Security Register #2	00h	0 0 1 0	0 0 0 0	Byte Address
Security Register #3	00h	0 0 1 1	0 0 0 0	Byte Address

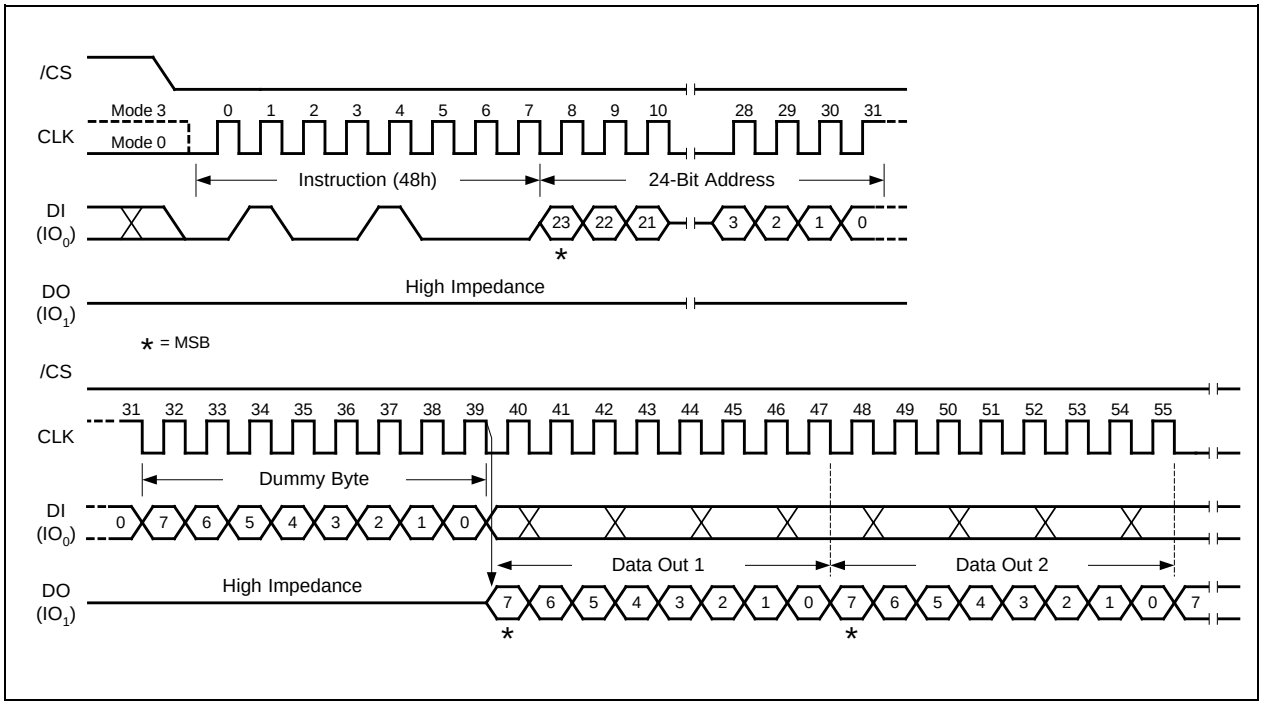


Figure 34. Read Security Registers Instruction

7.2.32 Individual Block/Sector Lock (36h)

The Individual Block/Sector Lock provides an alternative way to protect the memory array from adverse Erase/Program. In order to use the Individual Block/Sector Locks, the WPS bit in Status Register-3 must be set to 1. If WPS=0, the write protection will be determined by the combination of CMP, SEC, TB, BP[2:0] bits in the Status Registers. The Individual Block/Sector Lock bits are volatile bits. The default values after device power up or after a Reset are 1, so the entire memory array is being protected.

To lock a specific block or sector as illustrated in Figure 35, an Individual Block/Sector Lock command must be issued by driving /CS low, shifting the instruction code “36h” into the Data Input (DI) pin on the rising edge of CLK, followed by a 24-bit address and then driving /CS high. A Write Enable instruction must be executed before the device will accept the Individual Block/Sector Lock Instruction (Status Register bit WEL= 1).

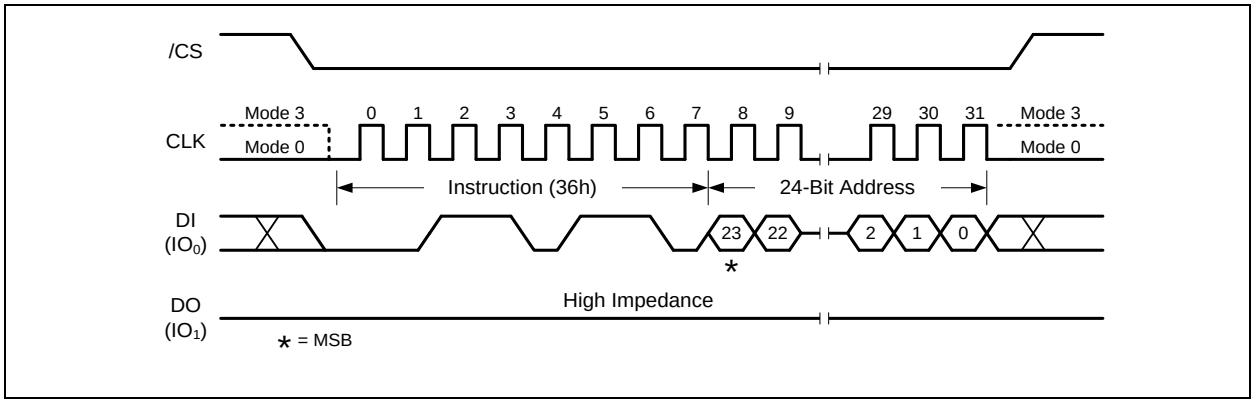


Figure 35. Individual Block/Sector Lock Instruction

7.2.33 Individual Block/Sector Unlock (39h)

The Individual Block/Sector Lock provides an alternative way to protect the memory array from adverse Erase/Program. In order to use the Individual Block/Sector Locks, the WPS bit in Status Register-3 must be set to 1. If WPS=0, the write protection will be determined by the combination of CMP, SEC, TB, BP[2:0] bits in the Status Registers. The Individual Block/Sector Lock bits are volatile bits. The default values after device power up or after a Reset are 1, so the entire memory array is being protected.

To unlock a specific block or sector as illustrated in Figure 36, an Individual Block/Sector Unlock command must be issued by driving /CS low, shifting the instruction code “39h” into the Data Input (DI) pin on the rising edge of CLK, followed by a 24-bit address and then driving /CS high. A Write Enable instruction must be executed before the device will accept the Individual Block/Sector Unlock Instruction (Status Register bit WEL= 1).

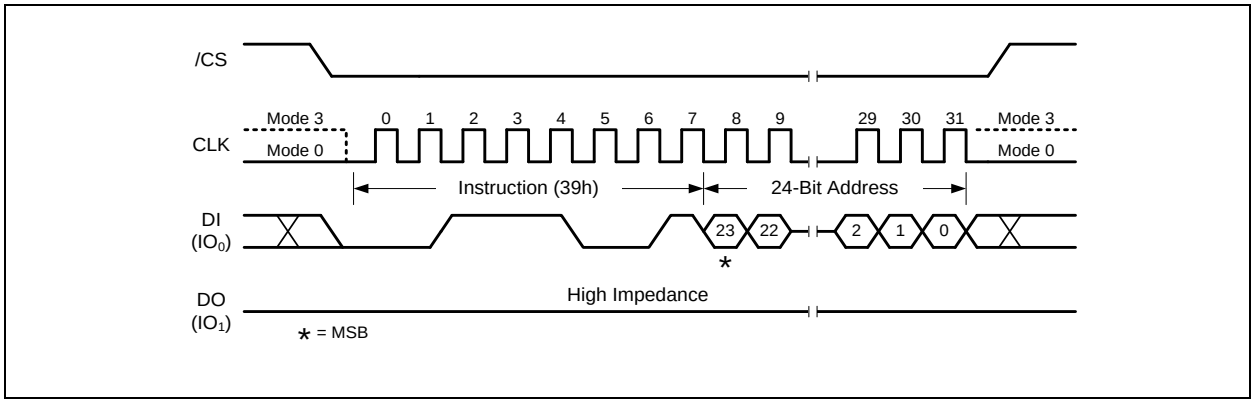


Figure 36. Individual Block Unlock Instruction

7.2.34 Read Block/Sector Lock (3Dh)

The Individual Block/Sector Lock provides an alternative way to protect the memory array from adverse Erase/Program. In order to use the Individual Block/Sector Locks, the WPS bit in Status Register-3 must be set to 1. If WPS=0, the write protection will be determined by the combination of CMP, SEC, TB, BP[2:0] bits in the Status Registers. The Individual Block/Sector Lock bits are volatile bits. The default values after device power up or after a Reset are 1, so the entire memory array is being protected.

To read out the lock bit value of a specific block or sector as illustrated in Figure 37, a Read Block/Sector Lock command must be issued by driving /CS low, shifting the instruction code “3Dh” into the Data Input (DI) pin on the rising edge of CLK, followed by a 24-bit address. The Block/Sector Lock bit value will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in Figure 55. If the least significant bit (LSB) is 1, the corresponding block/sector is locked; if LSB=0, the corresponding block/sector is unlocked, Erase/Program operation can be performed.

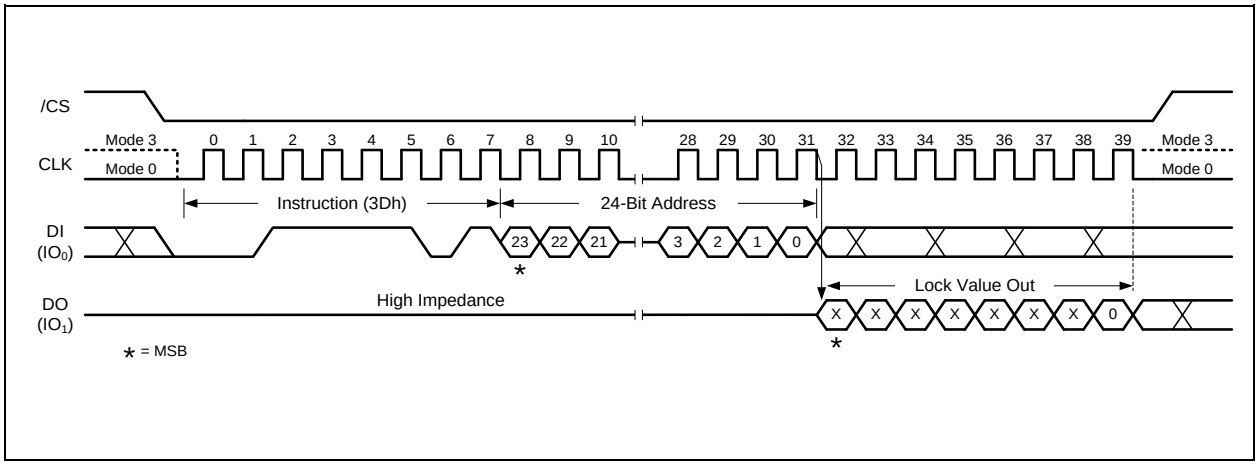


Figure 37. Read Block Lock Instruction

7.2.35 Global Block/Sector Lock (7Eh)

All Block/Sector Lock bits can be set to 1 by the Global Block/Sector Lock instruction. The command must be issued by driving /CS low, shifting the instruction code “7Eh” into the Data Input (DI) pin on the rising edge of CLK, and then driving /CS high. A Write Enable instruction must be executed before the device will accept the Global Block/Sector Lock Instruction (Status Register bit WEL= 1).

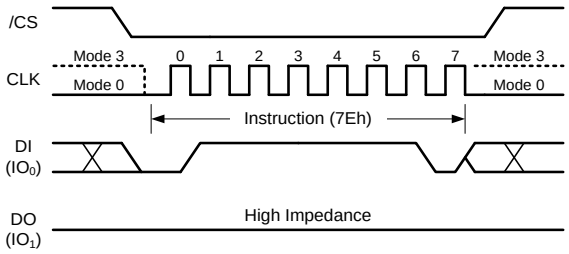


Figure 38. Global Block Lock Instruction for SPI Mode

7.2.36 Global Block/Sector Unlock (98h)

All Block/Sector Lock bits can be set to 0 by the Global Block/Sector Unlock instruction. The command must be issued by driving /CS low, shifting the instruction code “98h” into the Data Input (DI) pin on the rising edge of CLK, and then driving /CS high. A Write Enable instruction must be executed before the device will accept the Global Block/Sector Unlock Instruction (Status Register bit WEL= 1).

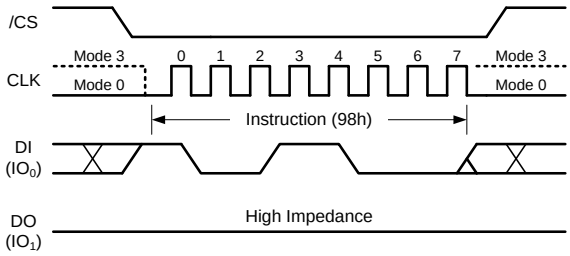


Figure 39. Global Block Unlock Instruction for SPI Mode

7.2.37 Enable Reset (66h) and Reset Device (99h)

Because of the small package and the limitation on the number of pins, the W25Q128JV provide a software Reset instruction instead of a dedicated RESET pin. Once the Reset instruction is accepted, any on-going internal operations will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch (WEL) status, Program/Erase Suspend status, Read parameter setting (P7-P0), and Wrap Bit setting (W6-W4).

“Enable Reset (66h)” and “Reset (99h)” instructions can be issued in SPI. To avoid accidental reset, both instructions must be issued in sequence. Any other commands other than “Reset (99h)” after the “Enable Reset (66h)” command will disable the “Reset Enable” state. A new sequence of “Enable Reset (66h)” and “Reset (99h)” is needed to reset the device. Once the Reset command is accepted by the device, the device will take approximately tRST=30us to reset. During this period, no command will be accepted.

Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the BUSY bit and the SUS bit in Status Register before issuing the Reset command sequence.

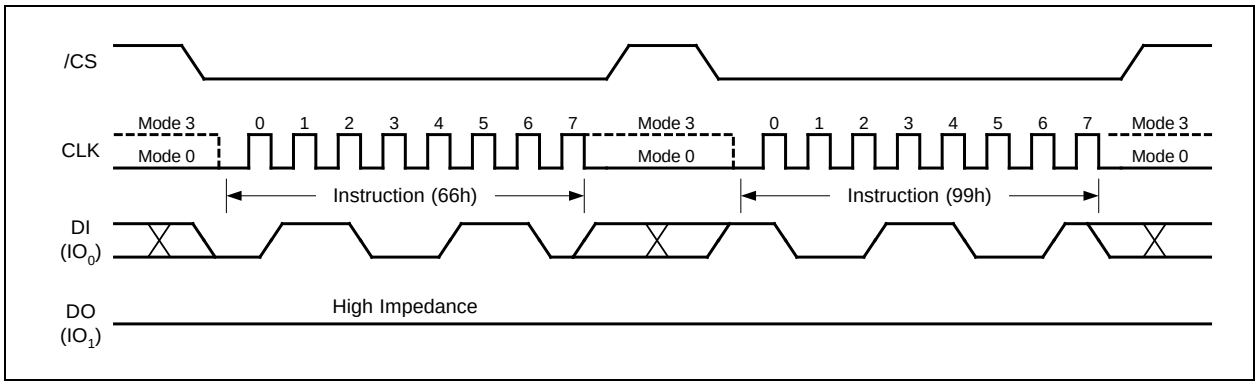


Figure 40. Enable Reset and Reset Instruction Sequence

8. ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings (1)

PARAMETERS	SYMBOL	CONDITIONS	RANGE	UNIT
Supply Voltage	VCC		–0.6 to 4.6	V
Voltage Applied to Any Pin	VIO	Relative to Ground	–0.6 to VCC+0.4	V
Transient Voltage on any Pin	VIOT	<20nS Transient Relative to Ground	–2.0V to VCC+2.0V	V
Storage Temperature	TSTG		–65 to +150	°C
Lead Temperature	TLEAD		See Note (2)	°C
Electrostatic Discharge Voltage	VESD	Human Body Model(3)	–2000 to +2000	V

Notes:

1. This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.
2. Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.
3. JEDEC Std JESD22-A114A (C1=100pF, R1=1500 ohms, R2=500 ohms).

8.2 Operating Ranges

PARAMETER	SYMBOL	CONDITIONS	SPEC		UNIT
			MIN	MAX	
Supply Voltage(1)	VCC	F_R = 133MHz, f_R = 50MHz	3.0	3.6	V
		F_R = 104MHz, f_R = 50MHz	2.7	3.0	V
Ambient Temperature, Operating	TA	Industrial	–40	+85	°C

Note:

1. VCC voltage during Read can operate across the min and max range but should not exceed ±10% of the programming (erase/write) voltage.

8.3 Power-Up Power-Down Timing and Requirements

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
VCC (min) to /CS Low	t_{VSL}(1)	20		µs
Time Delay Before Write Instruction	t_{PUW}(1)	5		ms
Write Inhibit Threshold Voltage	V_{WI}(1)	1.0	2.0	V

Note:

1. These parameters are characterized only.

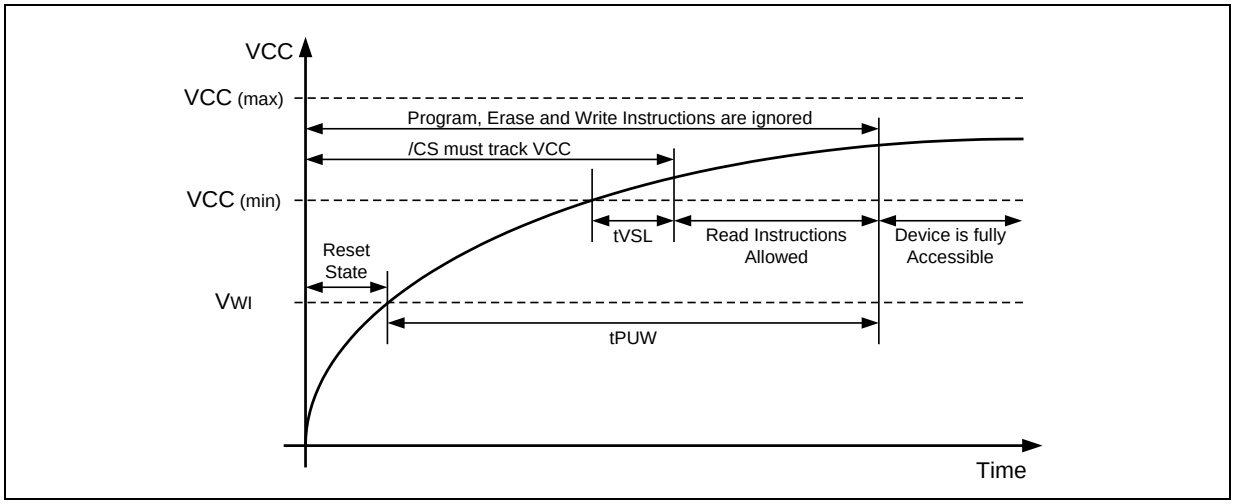


Figure 41a. Power-up Timing and Voltage Levels

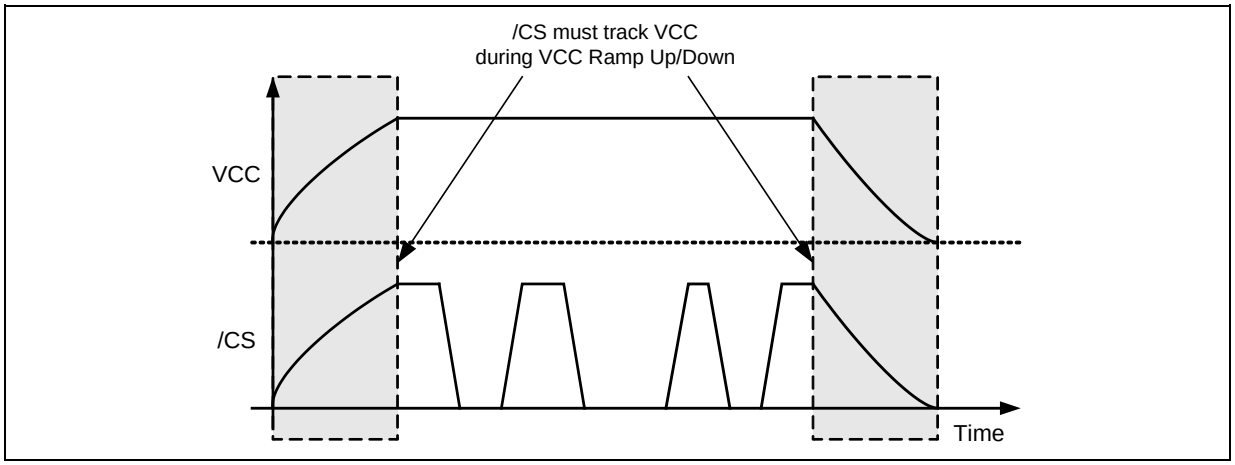


Figure 41b. Power-up, Power-Down Requirement

8.4 DC Electrical Characteristics-

PARAMETER	SYMBOL	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	
Input Capacitance	C_{IN}(1)	V_{IN} = 0V(1)			6	pF
Output Capacitance	Cout(1)	V_{OUT} = 0V(1)			8	pF
Input Leakage	I_{LI}				±2	µA
I/O Leakage	I_{LO}				±2	µA
Standby Current	I_{CC1}	/CS = VCC, VIN = GND or VCC		10	60	µA
Power-down Current	I_{CC2}	/CS = VCC, VIN = GND or VCC		1	20	µA
Current Read Data / Dual /Quad 50MHz(2)	I_{CC3}	C = 0.1 VCC / 0.9 VCC DO = Open			15	mA
Current Read Data / Dual /Quad 80MHz(2)	I_{CC3}	C = 0.1 VCC / 0.9 VCC DO = Open			18	mA
Current Read Data / Dual /Quad 104MHz(2)	I_{CC3}	C = 0.1 VCC / 0.9 VCC DO = Open			20	mA
Current Write Status Register	I_{CC4}	/CS = VCC		20	25	mA
Current Page Program	I_{CC5}	/CS = VCC		20	25	mA
Current Sector/Block Erase	I_{CC6}	/CS = VCC		20	25	mA
Current Chip Erase	I_{CC7}	/CS = VCC		20	25	mA
Input Low Voltage	V_{IL}		–0.5		VCC x 0.3	V
Input High Voltage	V_{IH}		VCC x 0.7		VCC + 0.4	V
Output Low Voltage	V_{OL}	I_{OL} = 100 µA			0.2	V
Output High Voltage	V_{OH}	I_{OH} = –100 µA	VCC – 0.2			V

Notes:

1. Tested on sample basis and specified through design and characterization data. TA = 25° C, VCC = 3.0V.
2. Checker Board Pattern.

8.5 AC Measurement Conditions

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
Load Capacitance	C_L		30	pF
Input Rise and Fall Times	T_R, T_F		5	ns
Input Pulse Voltages	V_{IN}	0.1 VCC to 0.9 VCC		V
Input Timing Reference Voltages	IN	0.3 VCC to 0.7 VCC		V
Output Timing Reference Voltages	OUT	0.5 VCC to 0.5 VCC		V

Note:

1. Output Hi-Z is defined as the point where data out is no longer driven.

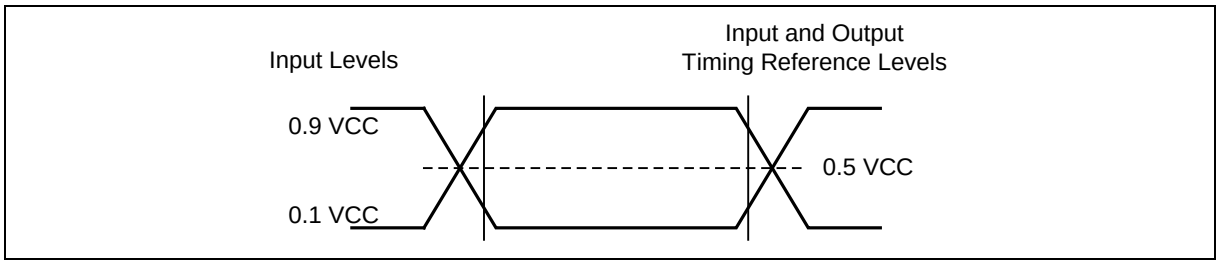


Figure 42. AC Measurement I/O Waveform

8.6 AC Electrical Characteristics(6)

DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
Clock frequency except for Read Data (03h) instructions (3.0V-3.6V)	F_R	f_{C1}	D.C.		133	MHz
Clock frequency except for Read Data (03h) instructions(2.7V-3.0V)	F_R	f_{C2}	D.C.		104	MHz
Clock frequency for Read Data instruction (03h)	f_R		D.C.		50	MHz
Clock High, Low Time for all instructions except for Read Data (03h)	t_{CLH}, t_{CLL}(1)		45% PC			ns
Clock High, Low Time for Read Data (03h) instruction	t_{CRLH}, t_{CRLL}(1)		45% PC			ns
Clock Rise Time peak to peak	t_{CLCH}(2)		0.1			V/ns
Clock Fall Time peak to peak	t_{CHCL}(2)		0.1			V/ns
/CS Active Setup Time relative to CLK	t_{SLCH}	t_{CSS}	5			ns
/CS Not Active Hold Time relative to CLK	t_{CHSL}		5			ns
Data In Setup Time	t_{DVCH}	t_{DSU}	2			ns
Data In Hold Time	t_{CHDX}	t_{DH}	3			ns
/CS Active Hold Time relative to CLK	t_{CHSH}		3			ns
/CS Not Active Setup Time relative to CLK	t_{SHCH}		3			ns
/CS Deselect Time (for Read)	t_{SHSL1}	t_{CSH}	10			ns
/CS Deselect Time (for Erase or Program or Write)	t_{SHSL2}	t_{CSH}	50			ns
Output Disable Time	t_{SHQZ}(2)	t_{DIS}			7	ns
Clock Low to Output Valid	t_{CLQV}	t_V			6	ns
Output Hold Time	t_{CLQX}	t_{HO}	1.5			ns

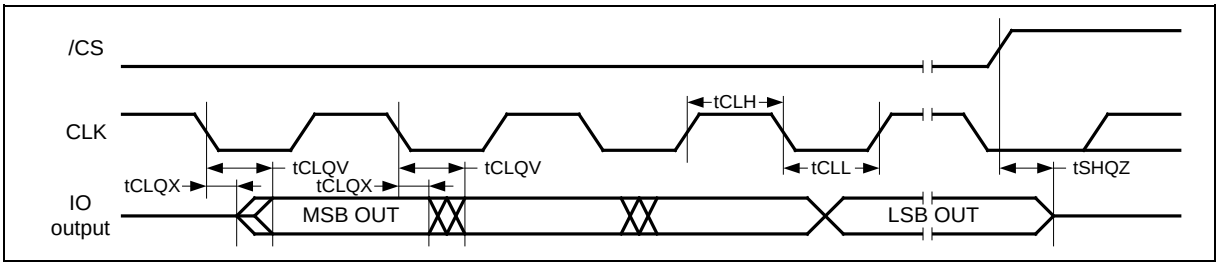
Continued – next page AC Electrical Characteristics (cont'd)

DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
/CS High to Power-down Mode	t_{DP}(2)				3	µs
/CS High to Standby Mode without ID Read	t_{RES1}(2)				3	µs
/CS High to Standby Mode with ID Read	t_{RES2}(2)				1.8	µs
/CS High to next Instruction after Suspend	t_{SUS}(2)				20	µs
/CS High to next Instruction after Reset	t_{RST}(2)				30	µs
/RESET pin Low period to reset the device	t_{RESET}(2)		1(4)			µs
Write Status Register Time	t_W			10	15	ms
Page Program Time	t_{PP}			0.7	3	ms
Sector Erase Time (4KB)	t_{SE}			45	400	ms
Block Erase Time (32KB)	t_{BE1}			120	1,600	ms
Block Erase Time (64KB)	t_{BE2}			150	2,000	ms
Chip Erase Time	t_{CE}			40	200	s

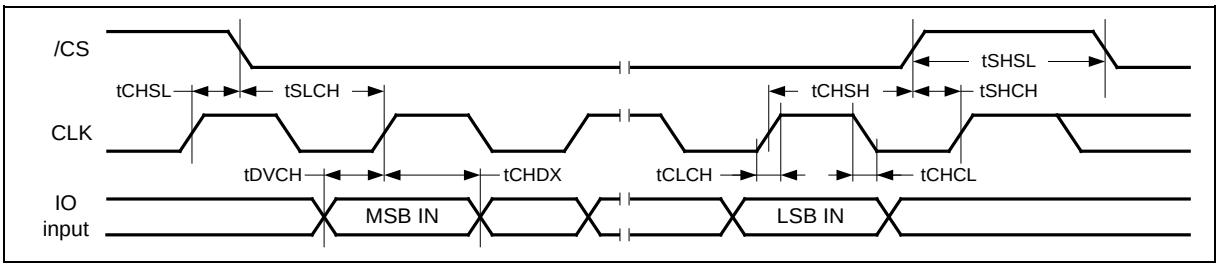
Notes:

1. Clock high or Clock low must be more than or equal to 45%Pc. Pc = 1/fc(max).
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Only applicable as a constraint for a Write Status Register instruction when SRP=1.
4. It's possible to reset the device with shorter t_{RESET} (as short as a few hundred ns), a 1us minimum is recommended to ensure reliable operation.
5. Tested on sample basis and specified through design and characterization data. T_A = 25° C, VCC = 3.0V, 25% driver strength.
6. 4-bytes address alignment for Quad Read

8.7 Serial Output Timing



8.8 Serial Input Timing



9. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A	01/09/2015		New Create Datasheet
B	11/04/2016		Removed “Preliminary”
C	08/23/2017	NA 17	Modified for MCP W25M121AV *SPISTACK* Datasheet Updated W25Q64JVxIQ SPISTACK Device ID
	08/25/2017	17	Changed device ID to 4018h from 4118h

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Featuring

3V 1G-BIT
SERIAL SLC NAND FLASH MEMORY WITH DUAL/QUAD SPI
BUFFER READ & CONTINUOUS READ

Publication Release Date: August 20, 2017
Revision I

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1. GENERAL DESCRIPTIONS

The W25N01GV (1G-bit) Serial SLC NAND Flash Memory provides a storage solution for systems with limited space, pins and power. The W25N SpiFlash family incorporates the popular SPI interface and the traditional large NAND non-volatile memory space. They are ideal for code shadowing to RAM, executing code directly from Dual/Quad SPI (XIP) and storing voice, text and data. The device operates on a single 2.7V to 3.6V power supply with current consumption as low as 25mA active and 10µA for standby. All W25N SpiFlash family devices are offered in space-saving packages which were impossible to use in the past for the typical NAND flash memory.

The W25N01GV 1G-bit memory array is organized into 65,536 programmable pages of 2,048-bytes each. The entire page can be programmed at one time using the data from the 2,048-Byte internal buffer. Pages can be erased in groups of 64 (128KB block erase). The W25N01GV has 1,024 erasable blocks.

The W25N01GV supports the standard Serial Peripheral Interface (SPI), Dual/Quad I/O SPI: Serial Clock, Chip Select, Serial Data I/O0 (DI), I/O1 (DO), I/O2 (/WP), and I/O3 (/HOLD). SPI clock frequencies of up to 104MHz are supported allowing equivalent clock rates of 208MHz (104MHz x 2) for Dual I/O and 416MHz (104MHz x 4) for Quad I/O when using the Fast Read Dual/Quad I/O instructions.

The W25N01GV provides a new Continuous Read Mode that allows for efficient access to the entire memory array with a single Read command. This feature is ideal for code shadowing applications.

A Hold pin, Write Protect pin and programmable write protection, provide further control flexibility. Additionally, the device supports JEDEC standard manufacturer and device ID, one 2,048-Byte Unique ID page, one 2,048-Byte parameter page and ten 2,048-Byte OTP pages. To provide better NAND flash memory manageability, user configurable internal ECC, bad block management are also available in W25N01GV.

2. FEATURES

- **New W25N Family of SpiFlash Memories**
  - W25N01GV: 1G-bit / 128M-byte
  - Standard SPI: CLK, /CS, DI, DO, /WP, /Hold
  - Dual SPI: CLK, /CS, IO_0, IO_1, /WP, /Hold
  - Quad SPI: CLK, /CS, IO_0, IO_1, IO_2, IO_3
  - Compatible SPI serial flash commands
- **Highest Performance Serial NAND Flash**
  - 104MHz Standard/Dual/Quad SPI clocks
  - 208/416MHz equivalent Dual/Quad SPI
  - 50MB/S continuous data transfer rate
  - Fast Program/Erase performance
  - More than 100,000 erase/program cycles
  - More than 10-year data retention
- **Efficient "Continuous Read Mode"(1)**
  - Alternative method to the Buffer Read Mode
  - No need to issue "Page Data Read" between Read commands
  - Allows direct read access to the entire array
- **Low Power, Wide Temperature Range**
  - Single 2.7 to 3.6V supply
  - 25mA active, 10µA standby current
  - -40°C to +85°C operating range
- **Flexible Architecture with 128KB blocks**
  - Uniform 128K-Byte Block Erase
  - Flexible page data load methods
- **Advanced Features**
  - On chip 1-Bit ECC for memory array
  - ECC status bits indicate ECC results
  - bad block management and LUT(2) access
  - Software and Hardware Write-Protect
  - Power Supply Lock-Down and OTP protection
  - 2KB Unique ID and 2KB parameter pages
  - Ten 2KB OTP pages(3)

Notes:

1. Only the Read command structures are different between the "Continuous Read Mode (BUF=0)" and the "Buffer Read Mode (BUF=1)", all other commands are identical. W25N01GVxxIG: Default BUF=1 after power up W25N01GVxxIT: Default BUF=0 after power up
2. LUT stands for Look-Up Table.
3. OTP pages can only be programmed.

3. PIN DESCRIPTIONS

3.1 Chip Select (/CS)

The SPI Chip Select (/CS) pin enables and disables device operation. When /CS is high the device is deselected and the Serial Data Output (DO, or IO0, IO1, IO2, IO3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When /CS is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, /CS must transition from high to low before a new instruction will be accepted. The /CS input must track the VCC supply level at power-up and power-down (see “Write Protection” and Figure 30b). If needed, a pull-up resistor on the /CS pin can be used to accomplish this.

3.2 Serial Data Input, Output and IOs (DI, DO and IO0, IO1, IO2, IO3)

The W25N01GV supports standard SPI, Dual SPI and Quad SPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge of CLK.

Dual and Quad SPI instructions use the bidirectional IO pins to serially write instructions, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK.

3.3 Write Protect (/WP)

The Write Protect (/WP) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register’s Block Protect bits BP[3:0] and Status Register Protect SRP bits SRP[1:0], a portion as small as 256K-Byte (2x128KB blocks) or up to the entire memory array can be hardware protected. The WP-E bit in the Protection Register (SR-1) controls the functions of the /WP pin.

When WP-E=0, the device is in the Software Protection mode that only SR-1 can be protected. The /WP pin functions as a data I/O pin for the Quad SPI operations, as well as an active low input pin for the Write Protection function for SR-1. Refer to section 7.1.3 for detail information.

When WP-E=1, the device is in the Hardware Protection mode that /WP becomes a dedicated active low input pin for the Write Protection of the entire device. If /WP is tied to GND, all “Write/Program/Erase” functions are disabled. The entire device (including all registers, memory array, OTP pages) will become read-only. Quad SPI read operations are also disabled when WP-E is set to 1.

3.4 HOLD (/HOLD)

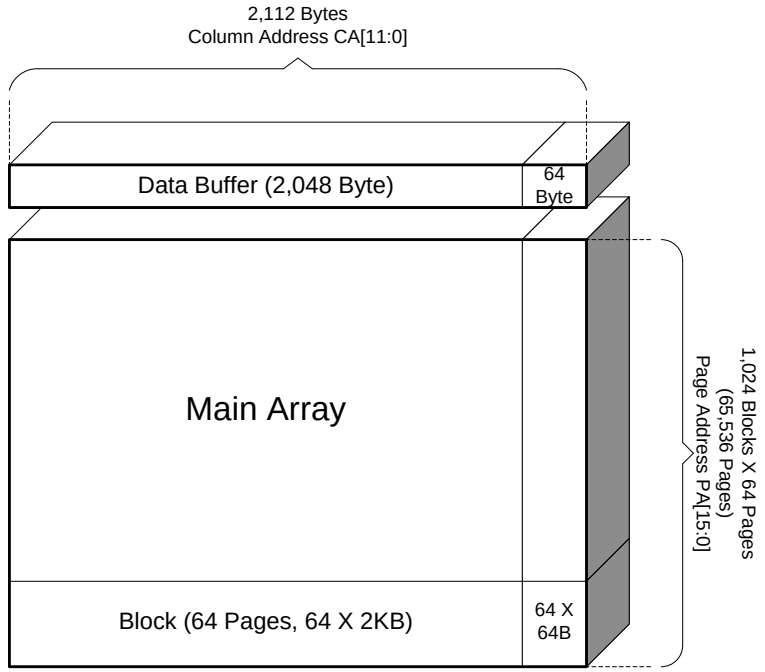
During Standard and Dual SPI operations, the /HOLD pin allows the device to be paused while it is actively selected. When /HOLD is brought low, while /CS is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don’t care). When /HOLD is brought high, device operation can resume. The /HOLD function can be useful when multiple devices are sharing the same SPI signals. The /HOLD pin is active low.

When a Quad SPI Read/Buffer Load command is issued, /HOLD pin will become a data I/O pin for the Quad operations and no HOLD function is available until the current Quad operation finishes. /HOLD (IO3) must be driven high by the host, or an external pull-up resistor must be placed on the PCB, in order to avoid allowing the /HOLD input to float.

3.5 Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Operations")

4. BLOCK DIAGRAM



Address Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SpiFlash (up to 128M-Bit)	X	X	X	X	X	X	X	X	64KB Block Addr (256 Blocks)								Page Address (256 Pages)								Byte Address (0-255 Byte)							
SpiFlash (up to 32G-Bit)	64KB Block Address																Page Address (256 Pages)								Byte Address (0-255 Byte)							
Serial NAND (1G-Bit)	X	X	X	X	**Page Address (PA) [15:0]**																**Column Address (CA) [11:0]**											
	X	X	X	X	128KB Block Addr (1024 Blocks)										Page Addr (64 Pages)						Ext	Byte Address (0-2047 Byte)										

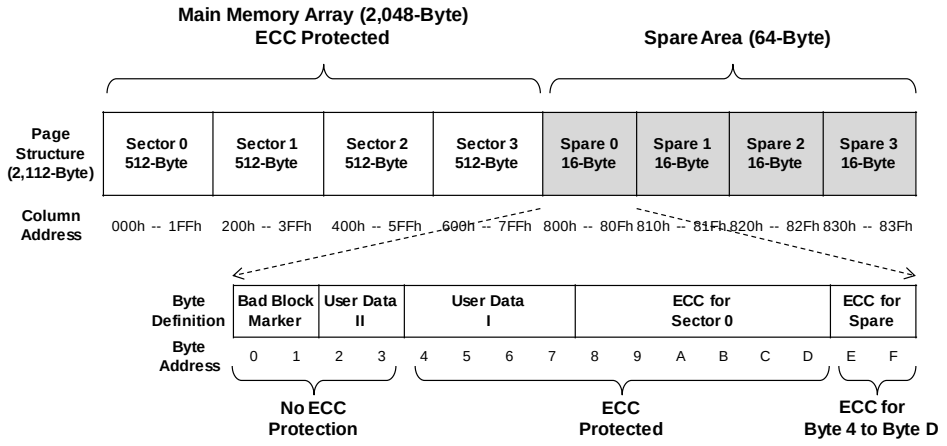


Figure 2. W25N01GV Flash Memory Architecture and Addressing

5. FUNCTIONAL DESCRIPTIONS

5.1 Device Operation Flow

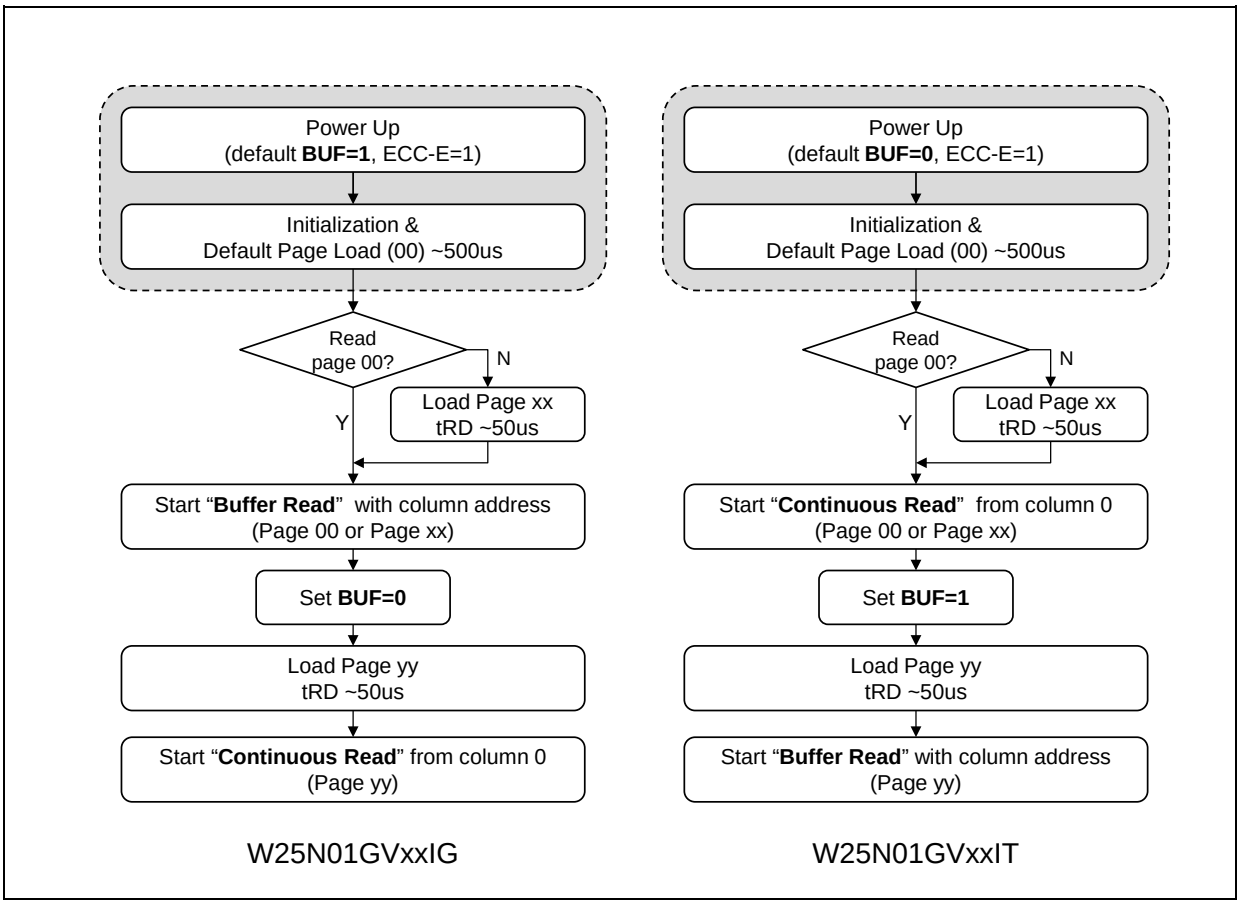


Figure 3. W25N01GV Flash Memory Operation Diagram

5.1.1 Standard SPI Instructions

The W25N01GV is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (/CS), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge of CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of /CS. For Mode 3, the CLK signal is normally high on the falling and rising edges of /CS.

5.1.2 Dual SPI Instructions

The W25N01GV supports Dual SPI operation when using instructions such as "Fast Read Dual Output (3Bh)" and "Fast Read Dual I/O (BBh)". These instructions allow data to be transferred to or from the device at two to three times the rate of ordinary Serial Flash devices. The Dual SPI Read instructions are ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed-critical

code directly from the SPI bus (XIP). When using Dual SPI instructions, the DI and DO pins become bidirectional I/O pins: IO0 and IO1.

5.1.3 Quad SPI Instructions

The W25N01GV supports Quad SPI operation when using instructions such as “Fast Read Quad Output (6Bh)”, “Fast Read Quad I/O (EBh)” and “Quad Program Data Load (32h/34h)”. These instructions allow data to be transferred to or from the device four to six times the rate of ordinary Serial Flash. The Quad Read instructions offer a significant improvement in continuous and random access transfer rates allowing fast code-shadowing to RAM or execution directly from the SPI bus (XIP). When using Quad SPI instructions the DI and DO pins become bidirectional IO0 and IO1, and the /WP and /HOLD pins become IO2 and IO3 respectively.

5.1.4 Hold Function

For Standard SPI and Dual SPI operations, the /HOLD signal allows the W25N01GV operation to be paused while it is actively selected (when /CS is low). The /HOLD function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, consider if the page buffer was only partially written when a priority interrupt requires use of the SPI bus. In this case the /HOLD function can save the state of the instruction and the data in the buffer so programming can resume where it left off once the bus is available again. The /HOLD function is only available for standard SPI and Dual SPI operation, not during Quad SPI. When a Quad SPI command is issued, /HOLD pin will act as a dedicated IO pin (IO3).

To initiate a /HOLD condition, the device must be selected with /CS low. A /HOLD condition will activate on the falling edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will activate after the next falling edge of CLK. The /HOLD condition will terminate on the rising edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will terminate after the next falling edge of CLK. During a /HOLD condition, the Serial Data Output (DO) is high impedance, and Serial Data Input (DI) and Serial Clock (CLK) are ignored. The Chip Select (/CS) signal should be kept active (low) for the full duration of the /HOLD operation to avoid resetting the internal logic state of the device.

5.2 Write Protection

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern, the W25N01GV provides several means to protect the data from inadvertent writes.

- Device resets when VCC is below threshold
- Write enable/disable instructions and automatic write disable after erase or program
- Software and Hardware (/WP pin) write protection using Protection Register (SR-1)
- Lock Down write protection for Protection Register (SR-1) until the next power-up
- One Time Program (OTP) write protection for memory array using Protection Register (SR-1)
- Hardware write protection using /WP pin when WP-E is set to 1

Upon power-up or at power-down, the W25N01GV will maintain a reset condition while VCC is below the threshold value of V_{WI}, (See Power-up Timing and Voltage Levels and Figure 30a). While reset, all operations are disabled and no instructions are recognized. During power-up and after the VCC voltage exceeds V_{WI}, all program and erase related instructions are further disabled for a time delay of t_{PUW}. This includes the Write Enable, Program Execute, Block Erase and the Write Status Register instructions. Note that the chip select pin (/CS) must track the VCC supply level at power-up until the VCC-min level and t_{VSL} time delay is reached, and it must also track the VCC supply level at power-down to prevent adverse command sequence. If needed a pull-up resister on /CS can be used to accomplish this.

After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a Program Execute or Block Erase instruction will be accepted. After completing a program or erase instruction the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (SRP0, SRP1) and Block Protect (TB, BP[3:0]) bits. These settings allow a portion or the entire memory array to be configured as read only. Used in conjunction with the Write Protect (/WP) pin, changes to the Status Register can be enabled or disabled under hardware control. See Protection Register section for further information.

The WP-E bit in Protection Register (SR-1) is used to enable the hardware protection. When WP-E is set to 1, bringing /WP low in the system will block any Write/Program/Erase command to the W25N01GV, the device will become read-only. The Quad SPI operations are also disabled when WP-E is set to 1.

6. PROTECTION, CONFIGURATION AND STATUS REGISTERS

Three Status Registers are provided for W25N01GV: Protection Register (SR-1), Configuration Register (SR-2) & Status Register (SR-3). Each register is accessed by Read Status Register and Write Status Register commands combined with 1-Byte Register Address respectively.

The Read Status Register instruction (05h / 0Fh) can be used to provide status on the availability of the flash memory array, whether the device is write enabled or disabled, the state of write protection, Read modes, Protection Register/OTP area lock status, Erase/Program results, and ECC usage/status. The Write Status Register instruction can be used to configure the device write protection features, Software/Hardware write protection, Read modes, enable/disable ECC, Protection Register/OTP area lock. Write access to the Status Register is controlled by the state of the non-volatile Status Register Protect bits (SRP0, SRP1), the Write Enable instruction, and when WP-E is set to 1, the /WP pin.

6.1 Protection Register / Status Register-1 (Volatile Writable, OTP lockable)

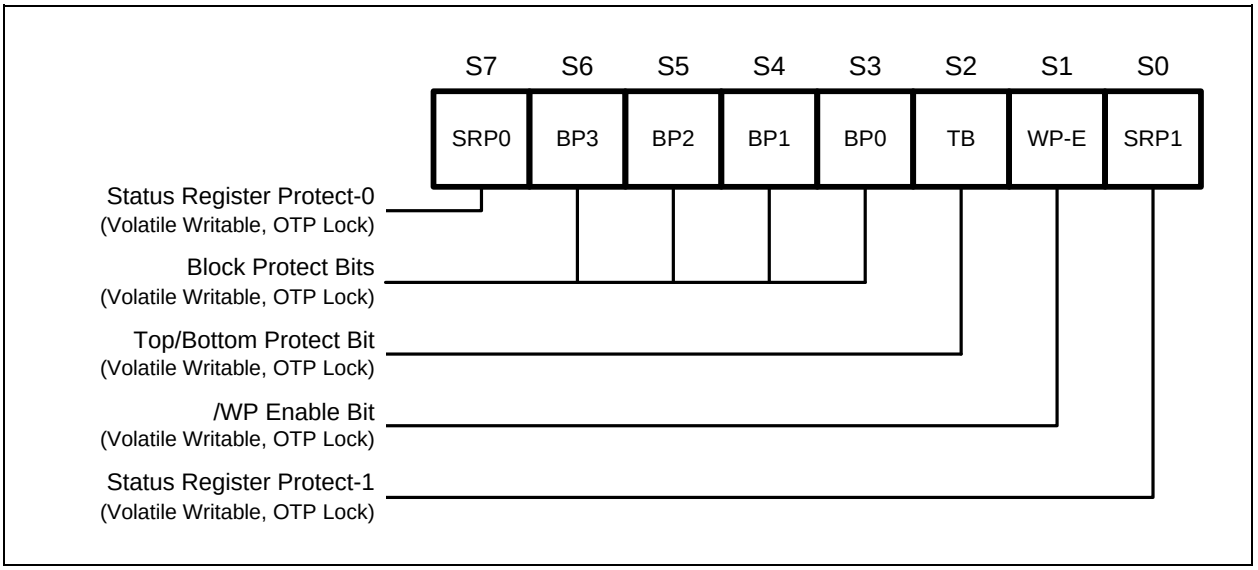


Figure 4a. Protection Register / Status Register-1 (Address Axh)

6.1.1 Block Protect Bits (BP3, BP2, BP1, BP0, TB) – *Volatile Writable, OTP lockable*

The Block Protect bits (BP3, BP2, BP1, BP0 and TB) are volatile read/write bits in the status register-1 (S6, S5, S4, S3 & S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction. All, none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection table). The default values for the Block Protection bits are 1 after power up to protect the entire array. If the SR1-L bit in the Configuration Register (SR-2) is set to 1, the default values will the values that are OTP locked.

6.1.2 Write Protection Enable Bit (WP-E) – *Volatile Writable, OTP lockable*

The Write Protection Enable bit (WP-E) is a volatile read/write bits in the status register-1 (S1). The WP-E bit, in conjunction with SRP1 & SRP0, controls the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable (OTP) protection, /WP pin functionality, and Quad SPI operation enable/disable. When WP-E = 0 (default value), the device is in Software Protection mode, /WP & /HOLD pins are multiplexed as IO pins, and Quad program/read functions are enabled all the time. When WP-E is set to 1, the device is in Hardware Protection mode, all Quad functions are disabled and /WP & /HOLD pins become dedicated control input pins.

6.1.3 Status Register Protect Bits (SRP1, SRP0) – *Volatile Writable, OTP lockable*

The Status Register Protect bits (SRP1 and SRP0) are volatile read/write bits in the status register (S0 and S7). The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable (OTP) protection.

Software Protection (Driven by Controller, Quad Program/Read is enabled)				
SRP1	**SRP0**	**WP-E**	**/WP / IO2**	**Descriptions**
0	0	0	X	No /WP functionality */WP pin will always function as IO2*
0	1	0	0	SR-1 cannot be changed (/WP = 0 during Write Status) */WP pin will function as IO2 for Quad operations*
0	1	0	1	SR-1 can be changed (/WP = 1 during Write Status) */WP pin will function as IO2 for Quad operations*
1	0	0	X	Power Lock Down(1) SR-1 */WP pin will always function as IO2*
1	1	0	X	Enter OTP mode to protect SR-1 (allow SR1-L=1) */WP pin will always function as IO2*

Hardware Protection (System Circuit / PCB layout, Quad Program/Read is disabled)				
SRP1	**SRP0**	**WP-E**	**/WP only**	**Descriptions**
0	X	1	VCC	SR-1 can be changed
1	0	1	VCC	Power Lock-Down(1) SR-1
1	1	1	VCC	Enter OTP mode to protect SR-1 (allow SR1-L=1)
X	X	1	GND	All "Write/Program/Erase" commands are blocked Entire device (SRs, Array, OTP area) is read-only

Notes:

1. When SRP1, SRP0 = (1, 0), a power-down, power-up cycle will change SRP1, SRP0 to (0, 0) state.

6.2 Configuration Register / Status Register-2 (Volatile Writable)

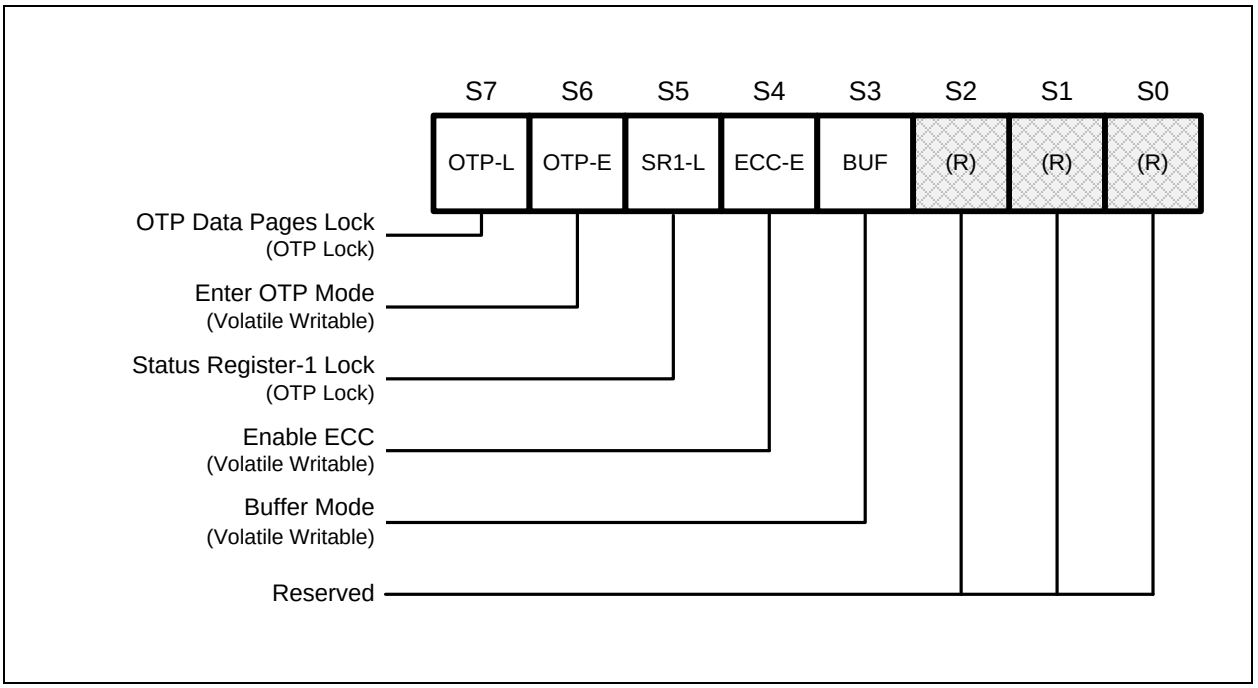


Figure 4b. Configuration Register / Status Register-2 (Address Bxh)

6.2.1 One Time Program Lock Bit (OTP-L) – *OTP lockable*

In addition to the main memory array, W25N01GV also provides an OTP area for the system to store critical data that cannot be changed once it's locked. The OTP area consists of 10 pages of 2,112-Byte each. The default data in the OTP area are FFh. Only Program command can be issued to the OTP area to change the data from "1" to "0", and data is not reversible ("0" to "1") by the Erase command. Once the correct data is programmed in and verified, the system developer can set OTP-L bit to 1, so that the entire OTP area will be locked to prevent further alteration to the data.

6.2.2 Enter OTP Access Mode Bit (OTP-E) – *Volatile Writable*

The OTP-E bit must be set to 1 in order to use the standard Program/Read commands to access the OTP area as well as to read the Unique ID / Parameter Page information. The default value after power up or a RESET command is 0.

6.2.3 Status Register-1 Lock Bit (SR1-L) – *OTP lockable*

The SR1-L lock bit is used to OTP lock the values in the Protection Register (SR-1). Depending on the settings in the SR-1, the device can be configured to have a portion of or up to the entire array to be write-protected, and the setting can be OTP locked by setting SR1-L bit to 1. SR1-L bit can only be set to 1 permanently when SRP1 & SRP0 are set to (1,1), and OTP Access Mode must be entered (OTP-E=1) to execute the programming. Please refer to 8.2.26 for detailed information.

6.2.4 ECC Enable Bit (ECC-E) – *Volatile Writable*

W25N01GV has a built-in ECC algorithm that can be used to preserve the data integrity. Internal ECC calculation is done during page programming, and the result is stored in the extra 64-Byte area for each page. During the data read operation, ECC engine will verify the data values according to the previously stored ECC information and to make necessary corrections if needed. The verification and correction status is indicated by the ECC Status Bits. ECC function is enabled by default when power on (ECC-E=1), and it will not be reset to 0 by the Device Reset command.

6.2.5 Buffer Read / Continuous Read Mode Bit (BUF) – *Volatile Writable*

W25N01GV provides two different modes for read operations, Buffer Read Mode (BUF=1) and Continuous Read Mode (BUF=0). Prior to any Read operation, a Page Data Read command is needed to initiate the data transfer from a specified page in the memory array to the Data Buffer. By default, after power up, the data in page 0 will be automatically loaded into the Data Buffer and the device is ready to accept any read commands.

The Buffer Read Mode (BUF=1) requires a Column Address to start outputting the existing data inside the Data Buffer, and once it reaches the end of the data buffer (Byte 2,111), DO (IO1) pin will become high-Z state.

The Continuous Read Mode (BUF=0) doesn't require the starting Column Address. The device will always start output the data from the first column (Byte 0) of the Data buffer, and once the end of the data buffer (Byte 2,048) is reached, the data output will continue through the next memory page. With Continuous Read Mode, it is possible to read out the entire memory array using a single read command. Please refer to respective command descriptions for the dummy cycle requirements for each read commands under different read modes.

For W25N01GVxxIG part number, the default value of BUF bit after power up is 1. BUF bit can be written to 0 in the Status Register-2 to perform the Continuous Read operation.

For W25N01GVxxIT part number, the default value of BUF bit after power up is 0. BUF bit can be written to 1 in the Status Register-2 to perform the Buffer Read operation.

BUF	ECC-E	Read Mode (Starting from Buffer)	ECC Status	Data Output Structure
1	0	Buffer Read	N/A	2,048 + 64
1	1	Buffer Read	Page based	2,048 + 64
0	0	Continuous Read	N/A	2,048
0	1	Continuous Read	Operation based	2,048

6.3 Status Register-3 (Status Only)

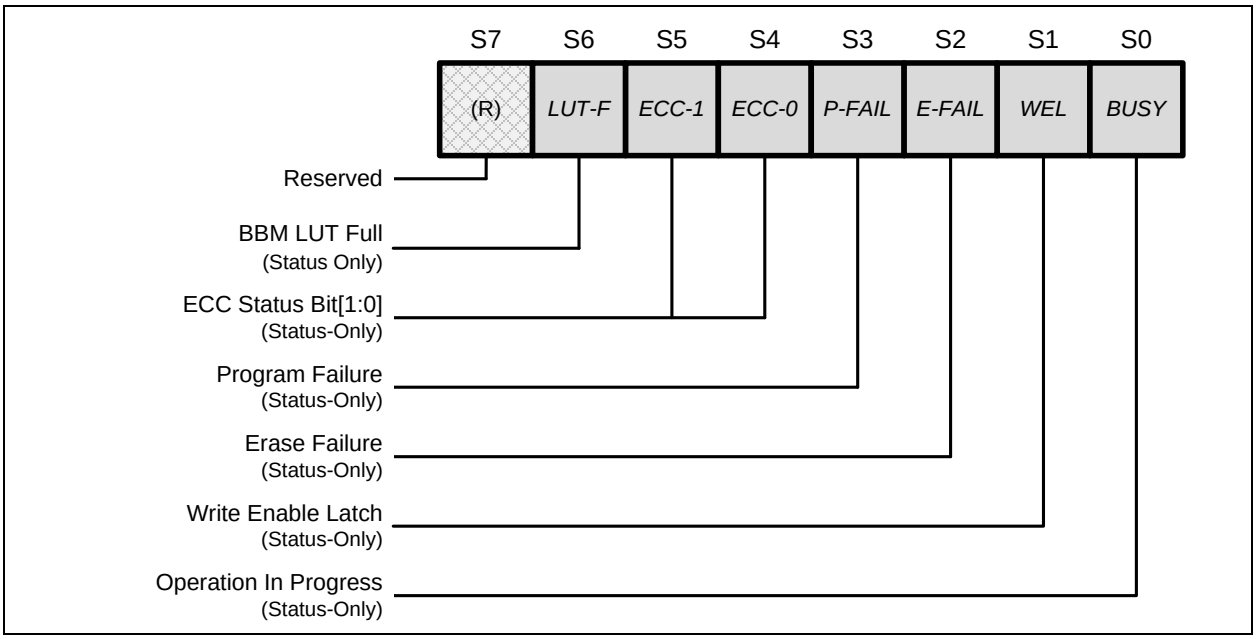


Figure 4c. Status Register-3 (Address Cxh)

6.3.1 Look-Up Table Full (LUT-F) – *Status Only*

To facilitate the NAND flash memory bad block management, the W25N01GV is equipped with an internal Bad Block Management Look-Up-Table (BBM LUT). Up to 20 bad memory blocks may be replaced by a good memory block respectively. The addresses of the blocks are stored in the internal Look-Up Table as Logical Block Address (LBA, the bad block) & Physical Block Address (PBA, the good block). The LUT-F bit indicates whether the 20 memory block links have been fully utilized or not. The default value of LUT-F is 0, once all 20 links are used, LUT-F will become 1, and no more memory block links may be established.

6.3.2 Cumulative ECC Status (ECC-1, ECC-0) – *Status Only*

ECC function is used in NAND flash memory to correct limited memory errors during read operations. The ECC Status Bits (ECC-1, ECC-0) should be checked after the completion of a Read operation to verify the data integrity. The ECC Status bits values are don't care if ECC-E=0. These bits will be cleared to 0 after a power cycle or a RESET command.

ECC Status		Descriptions
ECC-1	ECC-0	
0	0	Entire data output is **successful**, without any ECC correction.
0	1	Entire data output is **successful**, with 1~4 bit/page ECC corrections in either a single page or multiple pages.
1	0	Entire data output contains **more than 4 bits errors only in a single page which cannot be repaired by ECC**. In the Continuous Read Mode, an additional command can be used to read out the Page Address (PA) which had the errors.
1	1	Entire data output contains **more than 4 bits errors/page in multiple pages**. In the Continuous Read Mode, the additional command can only provide the last Page Address (PA) that had failures, the user cannot obtain the PAs for other failure pages. **Data is not suitable to use.**

Notes:

1. **ECC-1, ECC-0 = (1,1) is only applicable during Continuous Read operation (BUF=0).**

6.3.3 Program/Erase Failure (P-FAIL, E-FAIL) – *Status Only*

The Program/Erase Failure Bits are used to indicate whether the internally-controlled Program/Erase operation was executed successfully or not. These bits will also be set respectively when the Program or Erase command is issued to a locked or protected memory array or OTP area. Both bits will be cleared at the beginning of the Program Execute or Block Erase instructions as well as the device RESET instruction.

6.3.4 Write Enable Latch (WEL) – *Status Only*

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to 1 after executing a Write Enable Instruction. The WEL status bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Program Execute, Block Erase, Page Data Read and Program Execute for OTP pages.

6.3.5 Erase/Program In Progress (BUSY) – *Status Only*

BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is powering up or executing a Page Data Read, BBM Management, Program Execute, Block Erase, and Program Execute for OTP area, OTP Locking or after a Continuous Read instruction. During this time the device will ignore further instructions except for the Read Status Register and Read JEDEC ID instructions. When the program, erase or write status register instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions.

6.3.6 Reserved Bits – *Non Functional*

There are a few reserved Status Register bits that may be read out as a “0” or “1”. It is recommended to ignore the values of those bits. During a “Write Status Register” instruction, the Reserved Bits can be written as “0”, but there will not be any effects.

6.4 W25N01GV Status Register Memory Protection

STATUS REGISTER[1]					W25N01GV (1G-BIT / 128M-BYTE) MEMORY PROTECTION[2]			
TB	BP3	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED PAGE ADDRESS PA[15:0]	PROTECTED DENSITY	PROTECTED PORTION
X	0	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	1022 & 1023	FF80h - FFFFh	256KB	Upper 1/512
0	0	0	1	0	1020 thru 1023	FF00h - FFFFh	512KB	Upper 1/256
0	0	0	1	1	1016 thru 1023	FE00h - FFFFh	1MB	Upper 1/128
0	0	1	0	0	1008 thru 1023	FC00h - FFFFh	2MB	Upper 1/64
0	0	1	0	1	992 thru 1023	F800h - FFFFh	4MB	Upper 1/32
0	0	1	1	0	960 thru 1023	F000h - FFFFh	8MB	Upper 1/16
0	0	1	1	1	896 thru 1023	E000h - FFFFh	16MB	Upper 1/8
0	1	0	0	0	768 thru 1023	C000h - FFFFh	32MB	Upper 1/4
0	1	0	0	1	512 thru 1023	8000h - FFFFh	64MB	Upper 1/2
1	0	0	0	1	0 & 1	0000h – 007Fh	256KB	Lower 1/512
1	0	0	1	0	0 thru 3	0000h - 00FFh	512KB	Lower 1/256
1	0	0	1	1	0 thru 7	0000h - 01FFh	1MB	Lower 1/128
1	0	1	0	0	0 thru 15	0000h - 03FFh	2MB	Lower 1/64
1	0	1	0	1	0 thru 31	0000h - 07FFh	4MB	Lower 1/32
1	0	1	1	0	0 thru 63	0000h - 0FFFh	8MB	Lower 1/16
1	0	1	1	1	0 thru 127	0000h - 1FFFh	16MB	Lower 1/8
1	1	0	0	0	0 thru 255	0000h - 3FFFh	32MB	Lower 1/4
1	1	0	0	1	0 thru 511	0000h - 7FFFh	64MB	Lower 1/2
X	1	0	1	X	0 thru 1023	0000h - FFFFh	128MB	ALL
X	1	1	X	X	0 thru 1023	0000h - FFFFh	128MB	ALL

Notes:

1. X = don't care
2. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

7. INSTRUCTIONS

The Standard/Dual/Quad SPI instruction set of the W25N01GV consists of 27 basic instructions that are fully controlled through the SPI bus (see Instruction Set Table1, 2). Instructions are initiated with the falling edge of Chip Select (/CS). The first byte of data clocked into the DI input provides the instruction code. Data on the DI input is sampled on the rising edge of clock with most significant bit (MSB) first.

Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don't care), and in some cases, a combination. Instructions are completed with the rising edge of edge /CS. Clock relative timing diagrams for each instruction are included in Figures 5 through 29. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte boundary (/CS driven high after a full 8-bits have been clocked) otherwise the instruction will be ignored. This feature further protects the device from inadvertent writes. Additionally, while the device is performing Program or Erase operation, BBM management, Page Data Read or OTP locking operations, BUSY bit will be high, and all instructions except for Read Status Register or Read JEDEC ID will be ignored until the current operation cycle has completed.

7.1 Device ID and Instruction Set Tables

7.1.1 Manufacturer and Device Identification

MANUFACTURER ID	**(MF7 - MF0)**
Winbond Serial Flash	EFh
Device ID	**(ID15 - ID0)**
W25N01GV – SPISTACK®	AB21h

7.1.2 Instruction Set Table 1 (Continuous Read, BUF = 0, xxIT Default Power Up Mode)(11)

Commands	OpCode	Byte2	Byte3	Byte4	Byte5	Byte6	Byte7	Byte8	Byte9
Device RESET	**FFh**								
JEDEC ID	**9Fh**	Dummy	***EFh***	***AAh***	***21h***				
Read Status Register	**0Fh / 05h**	SR Addr	***S7-0***	***S7-0***	***S7-0***	***S7-0***	***S7-0***	***S7-0***	***S7-0***
Write Status Register	**1Fh / 01h**	SR Addr	S7-0						
Write Enable	**06h**								
Write Disable	**04h**								
BB Management (Swap Blocks)	**A1h**	LBA	LBA	PBA	PBA				
Read BBM LUT	**A5h**	Dummy	***LBA0***	***LBA0***	***PBA0***	***PBA0***	***LBA1***	***LBA1***	***PBA1***
Last ECC failure Page Address	**A9h**	Dummy	***PA15-8***	***PA7-0***					
Block Erase	**D8h**	Dummy	**PA15-8**	**PA7-0**					
Program Data Load (Reset Buffer)	**02h**	**CA15-8**	**CA7-0**	Data-0	Data-1	Data-2	Data-3	Data-4	Data-5
Random Program Data Load	**84h**	**CA15-8**	**CA7-0**	Data-0	Data-1	Data-2	Data-3	Data-4	Data-5
Quad Program Data Load (Reset Buffer)	**32h**	**CA15-8**	**CA7-0**	Data-0 / 4	Data-1 / 4	Data-2 / 4	Data-3 / 4	Data-4 / 4	Data-5 / 4
Random Quad Program Data Load	**34h**	**CA15-8**	**CA7-0**	Data-0 / 4	Data-1 / 4	Data-2 / 4	Data-3 / 4	Data-4 / 4	Data-5 / 4
Program Execute	**10h**	Dummy	**PA15-8**	**PA7-0**					
Page Data Read	**13h**	Dummy	**PA15-8**	**PA7-0**					
Read	**03h**	Dummy	Dummy	Dummy	***D7-0***	***D7-0***	***D7-0***	***D7-0***	***D7-0***
Fast Read	**0Bh**	Dummy	Dummy	Dummy	Dummy	***D7-0***	***D7-0***	***D7-0***	***D7-0***
Fast Read with 4-Byte Address	**0Ch**	Dummy	Dummy	Dummy	Dummy	Dummy	***D7-0***	***D7-0***	***D7-0***
Fast Read Dual Output	**3Bh**	Dummy	Dummy	Dummy	Dummy	***D7-0 / 2***	***D7-0 / 2***	***D7-0 / 2***	***D7-0 / 2***
Fast Read Dual Output with 4-Byte Address	**3Ch**	Dummy	Dummy	Dummy	Dummy	Dummy	***D7-0 / 2***	***D7-0 / 2***	***D7-0 / 2***
Fast Read Quad Output	**6Bh**	Dummy	Dummy	Dummy	Dummy	***D7-0 / 4***	***D7-0 / 4***	***D7-0 / 4***	***D7-0 / 4***
Fast Read Quad Output with 4-Byte Address	**6Ch**	Dummy	Dummy	Dummy	Dummy	Dummy	***D7-0 / 4***	***D7-0 / 4***	***D7-0 / 4***
Fast Read Dual I/O	**BBh**	Dummy / 2	Dummy / 2	Dummy / 2	Dummy / 2	***D7-0 / 2***	***D7-0 / 2***	***D7-0 / 2***	***D7-0 / 2***
Fast Read Dual I/O with 4-Byte Address	**BCh**	Dummy / 2	Dummy / 2	Dummy / 2	Dummy / 2	Dummy / 2	***D7-0 / 2***	***D7-0 / 2***	***D7-0 / 2***
Fast Read Quad I/O	**EBh**	Dummy / 4	Dummy / 4	Dummy / 4	Dummy / 4	Dummy / 4	Dummy / 4	***D7-0 / 4***	***D7-0 / 4***
Fast Read Quad I/O with 4-Byte Address	**ECh**	Dummy / 4	Dummy / 4	Dummy / 4	Dummy / 4	Dummy / 4	Dummy / 4	Dummy / 4	***D7-0 / 4***

7.1.3 Instruction Set Table 2 (Buffer Read, BUF = 1, xxIG Default Power Up Mode)(12)

Commands	OpCode	Byte2	Byte3	Byte4	Byte5	Byte6	Byte7	Byte8	Byte9
Device RESET	**FFh**								
JEDEC ID	**9Fh**	Dummy	***EFh***	***AAh***	***21h***				
Read Status Register	**0Fh / 05h**	SR Addr	***S7-0***	***S7-0***	***S7-0***	***S7-0***	***S7-0***	***S7-0***	***S7-0***
Write Status Register	**1Fh / 01h**	SR Addr	S7-0						
Write Enable	**06h**								
Write Disable	**04h**								
BB Management (Swap Blocks)	**A1h**	LBA	LBA	PBA	PBA				
Read BBM LUT	**A5h**	Dummy	***LBA0***	***LBA0***	***PBA0***	***PBA0***	***LBA1***	***LBA1***	***PBA1***
Last ECC failure Page Address	**A9h**	Dummy	***PA15-8***	***PA7-0***					
Block Erase	**D8h**	Dummy	**PA15-8**	**PA7-0**					
Program Data Load (Reset Buffer)	**02h**	**CA15-8**	**CA7-0**	Data-0	Data-1	Data-2	Data-3	Data-4	Data-5
Random Program Data Load	**84h**	**CA15-8**	**CA7-0**	Data-0	Data-1	Data-2	Data-3	Data-4	Data-5
Quad Program Data Load (Reset Buffer)	**32h**	**CA15-8**	**CA7-0**	Data-0 / 4	Data-1 / 4	Data-2 / 4	Data-3 / 4	Data-4 / 4	Data-5 / 4
Random Quad Program Data Load	**34h**	**CA15-8**	**CA7-0**	Data-0 / 4	Data-1 / 4	Data-2 / 4	Data-3 / 4	Data-4 / 4	Data-5 / 4
Program Execute	**10h**	Dummy	**PA15-8**	**PA7-0**					
Page Data Read	**13h**	Dummy	**PA15-8**	**PA7-0**					
Read	**03h**	**CA15-8**	**CA7-0**	Dummy	***D7-0***	***D7-0***	***D7-0***	***D7-0***	***D7-0***
Fast Read	**0Bh**	**CA15-8**	**CA7-0**	Dummy	***D7-0***	***D7-0***	***D7-0***	***D7-0***	***D7-0***
Fast Read with 4-Byte Address	**0Ch**	**CA15-8**	**CA7-0**	Dummy	Dummy	Dummy	***D7-0***	***D7-0***	***D7-0***
Fast Read Dual Output	**3Bh**	**CA15-8**	**CA7-0**	Dummy	***D7-0 / 2***	***D7-0 / 2***	***D7-0 / 2***	***D7-0 / 2***	***D7-0 / 2***
Fast Read Dual Output with 4-Byte Address	**3Ch**	**CA15-8**	**CA7-0**	Dummy	Dummy	Dummy	***D7-0 / 2***	***D7-0 / 2***	***D7-0 / 2***
Fast Read Quad Output	**6Bh**	**CA15-8**	**CA7-0**	Dummy	***D7-0 / 4***	***D7-0 / 4***	***D7-0 / 4***	***D7-0 / 4***	***D7-0 / 4***
Fast Read Quad Output with 4-Byte Address	**6Ch**	**CA15-8**	**CA7-0**	Dummy	Dummy	Dummy	***D7-0 / 4***	***D7-0 / 4***	***D7-0 / 4***
Fast Read Dual I/O	**BBh**	**CA15-8 / 2**	**CA7-0 / 2**	Dummy / 2	***D7-0 / 2***	***D7-0 / 2***	***D7-0 / 2***	***D7-0 / 2***	***D7-0 / 2***
Fast Read Dual I/O with 4-Byte Address	**BCh**	**CA15-8 / 2**	**CA7-0 / 2**	Dummy / 2	Dummy / 2	Dummy / 2	***D7-0 / 2***	***D7-0 / 2***	***D7-0 / 2***
Fast Read Quad I/O	**EBh**	**CA15-8 / 4**	**CA7-0 / 4**	Dummy / 4	Dummy / 4	***D7-0 / 4***	***D7-0 / 4***	***D7-0 / 4***	***D7-0 / 4***
Fast Read Quad I/O with 4-Byte Address	**ECh**	**CA15-8 / 4**	**CA7-0 / 4**	Dummy / 4	Dummy / 4	Dummy / 4	Dummy / 4	Dummy / 4	***D7-0 / 4***

Notes:

1. ***Output*** designates data output from the device.

2. Column Address (CA) only requires CA[11:0], CA[15:12] are considered as dummy bits.

3. Page Address (PA) requires 16 bits. PA[15:6] is the address for 128KB blocks (total 1,024 blocks), PA[5:0] is the address for 2KB pages (total 64 pages for each block).

4. Logical and Physical Block Address (LBA & PBA) each consists of 16 bits. LBA[9:0] & PBA[9:0] are effective Block Addresses. LBA[15:14] is used for additional information.

5. Status Register Addresses:

Status Register 1 / Protection Register:	Addr = Axh
Status Register 2 / Configuration Register:	Addr = Bxh
Status Register 3 / Status Register:	Addr = Cxh

6. Dual SPI Address Input (**CA15-8 / 2** and **CA7-0 / 2**) format:

IO0 =	x,	x,	CA10,	CA8,	CA6,	CA4,	CA2,	CA0
IO1 =	x,	x,	CA11,	CA9,	CA7,	CA5,	CA3,	CA1

7. Dual SPI Data Output (***D7-0 / 2***) format:

IO0 =	D6,	D4,	D2,	D0,	……
IO1 =	D7,	D5,	D3,	D1,	……

8. Quad SPI Address Input (**CA15-8 / 4** and **CA7-0 / 4**) format:

IO0 =	x,	CA8,	CA4,	CA0
IO1 =	x,	CA9,	CA5,	CA1
IO2 =	x,	CA10,	CA6,	CA2
IO3 =	x,	CA11,	CA7,	CA3

9. Quad SPI Data Input/Output (***D7-0 / 4***) format:

IO0 =	D4,	D0,	……
IO1 =	D5,	D1,	……
IO2 =	D6,	D2,	……
IO3 =	D7,	D3,	……

10. All Quad Program/Read commands are disabled when WP-E bit is set to 1 in the Protection Register.

11. For all Read operations in the Continuous Read Mode, once the /CS signal is brought to high to terminate the read operation, the device will still remain busy for ~5us (BUSY=1), and all the data inside the Data buffer will be lost and un-reliable to use. A new Page Data Read instruction must be issued to reload the correct page data into the Data Buffer.

12. For all Read operations in the Buffer Read Mode, as soon as /CS signal is brought to high to terminate the read operation, the device will be ready to accept new instructions and all the data inside the Data Buffer will remain unchanged from the previous Page Data Read instruction.

7.2 Instruction Descriptions

7.2.1 Device Reset (FFh)

Because of the small package and the limitation on the number of pins, the W25N01GV provide a software Reset instruction instead of a dedicated RESET pin. Once the Reset instruction is accepted, any on-going internal operations will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits. Once the Reset command is accepted by the device, the device will take approximately tRST to reset, depending on the current operation the device is performing, tRST can be 5us~500us. During this period, no command will be accepted.

Data corruption may happen if there is an on-going internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the BUSY bit in Status Register before issuing the Reset command.

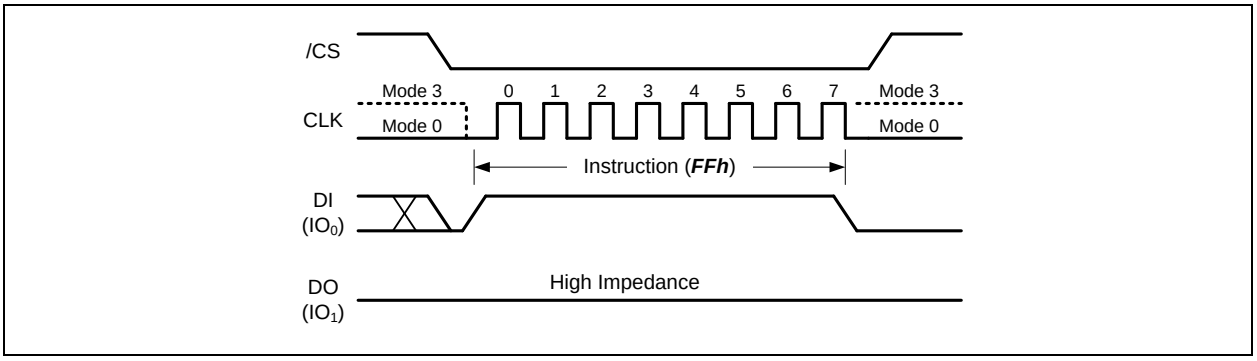


Figure 5. Device Reset Instruction

Register	Address	Bits	Shipment Default	Power Up after LUT is full	Power Up after OTP area locked	Power Up after SR-1 locked	After Reset command (FFh)
Protection Register	Axh	BP[3:0], TB	1111 1	1111 1	1111 1	xxxx x (locked)	No Change
		SRP[1:0]	0 0	0 0	0 0	1 1 (locked)	No Change
		WP-E	0	0	0	x (locked)	No Change
Configuration Register	Bxh	OTP-L	0	0	1	0	Clear to 0 before OTP set
		OTP-E	0	0	0	0	0
		SR1-L	0	0	0	1	Clear to 0 before OTP set
		ECC-E	1	1	1	1	No Change
		BUF (xxIG)	1	1	1	1	No Change
		BUF (xxIT)	0	0	0	0	No Change
Status Register	Cxh	LUT-F	0	1	0	0	No Change
		ECC-1	0	0	0	0	0
		ECC-0	0	0	0	0	0
		P-FAIL	0	0	0	0	0
		E-FAIL	0	0	0	0	0
		WEL	0	0	0	0	0
		BUSY	1 during tRST => 0	1 during tRST => 0	1 during tRST => 0	1 during tRST => 0	1 during tRST => 0

Default values of the Status Registers after power up and Device Reset

7.2.2 Read JEDEC ID (9Fh)

The Read JEDEC ID instruction is compatible with the JEDEC standard for SPI compatible serial memories that was adopted in 2003. The instruction is initiated by driving the /CS pin low and shifting the instruction code “9Fh” followed by 8 dummy clocks. The JEDEC assigned Manufacturer ID byte for Winbond (EFh) and two Device ID bytes are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 6. For memory type and capacity values refer to Manufacturer and Device Identification table.

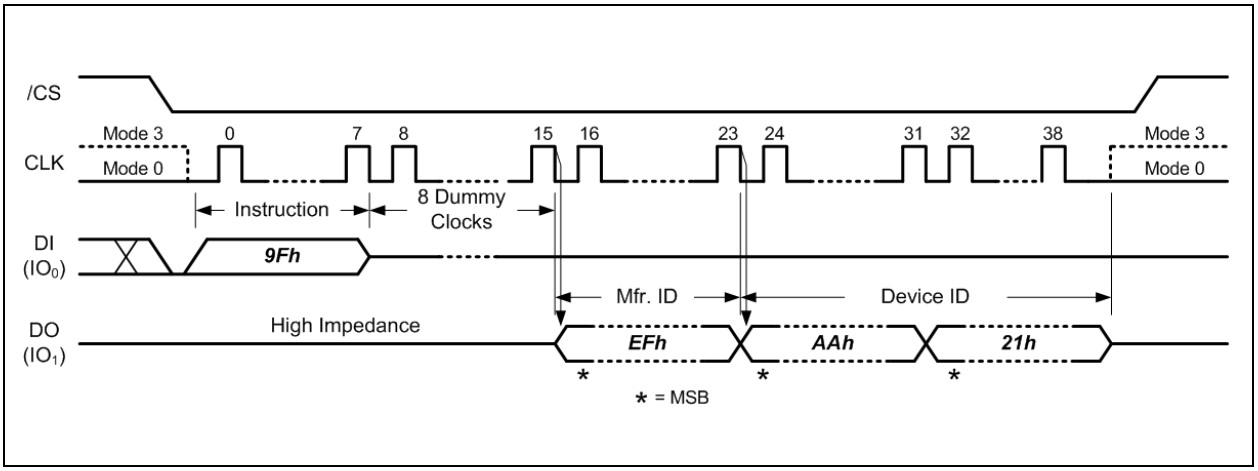


Figure 6. Read JEDEC ID Instruction

7.2.3 Read Status Register (0Fh / 05h)

The Read Status Register instructions allow the 8-bit Status Registers to be read. The instruction is entered by driving /CS low and shifting the instruction code “0Fh or 05h” into the DI pin on the rising edge of CLK followed by an 8-bit Status Register Address. The status register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in Figure 7. Refer to section 7.1-3 for Status Register descriptions.

The Read Status Register instruction may be used at any time, even while a Program or Erase cycle is in progress. This allows the BUSY status bit to be checked to determine when the cycle is complete and if the device can accept another instruction. The Status Register can be read continuously. The instruction is completed by driving /CS high.

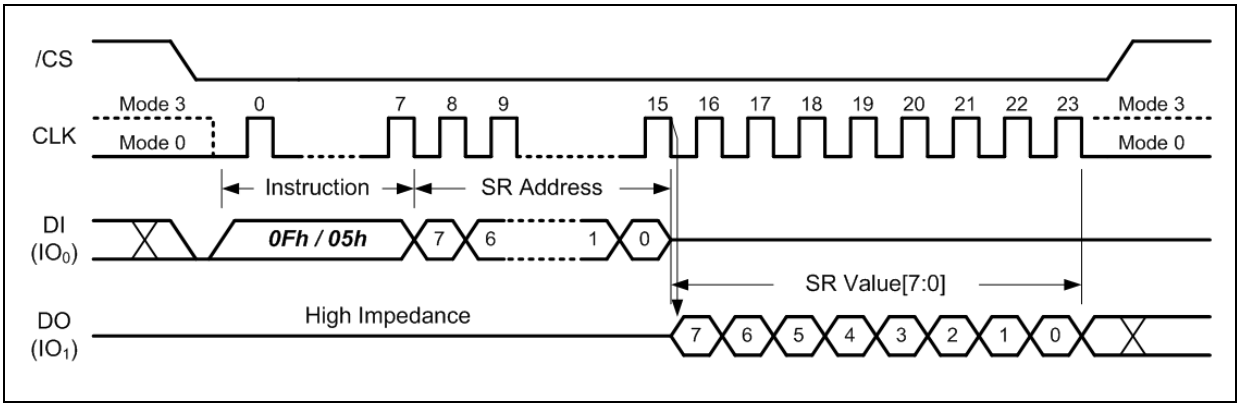


Figure 7. Read Status Register Instruction

7.2.4 Write Status Register (1Fh / 01h)

The Write Status Register instruction allows the Status Registers to be written. The writable Status Register bits include: SRP[1:0], TB, BP[3:0] and WP-E bit in Status Register-1; OTP-L, OTP-E, SR1-L, ECC-E and BUF bit in Status Register-2. All other Status Register bit locations are read-only and will not be affected by the Write Status Register instruction.

To write the Status Register bits, the instruction is entered by driving /CS low, sending the instruction code "1Fh or 01h", followed by an 8-bit Status Register Address, and then writing the status register data byte as illustrated in Figure 8.

Refer to section 7.1-3 for Status Register descriptions. After power up, factory default for BP[3:0], TB, ECC-E bits are 1, while other bits are 0.

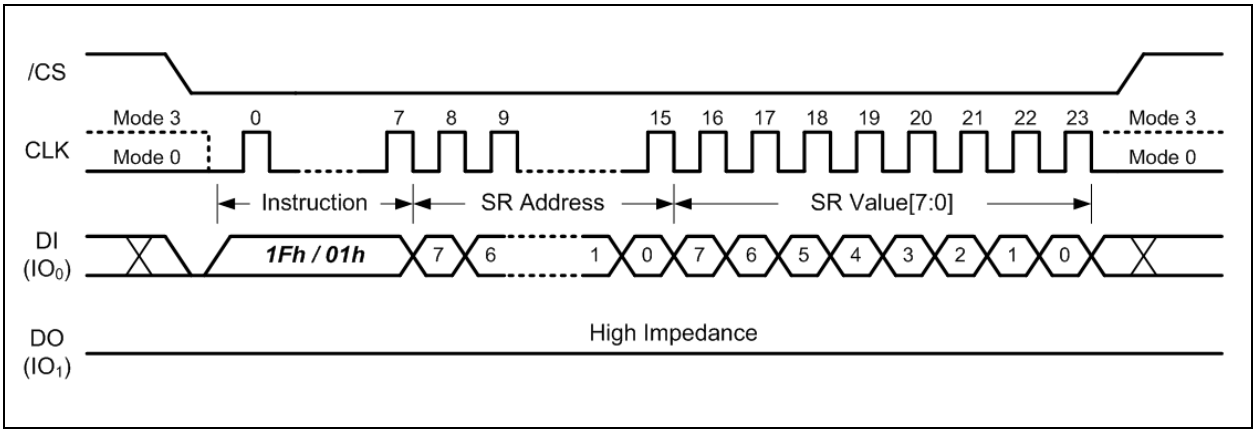


Figure 8. Write Status Register-1/2/3 Instruction

7.2.5 Write Enable (06h)

The Write Enable instruction (Figure 9) sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Page Program, Quad Page Program and Block Erase instruction. The Write Enable instruction is entered by driving /CS low, shifting the instruction code “06h” into the Data Input (DI) pin on the rising edge of CLK, and then driving /CS high.

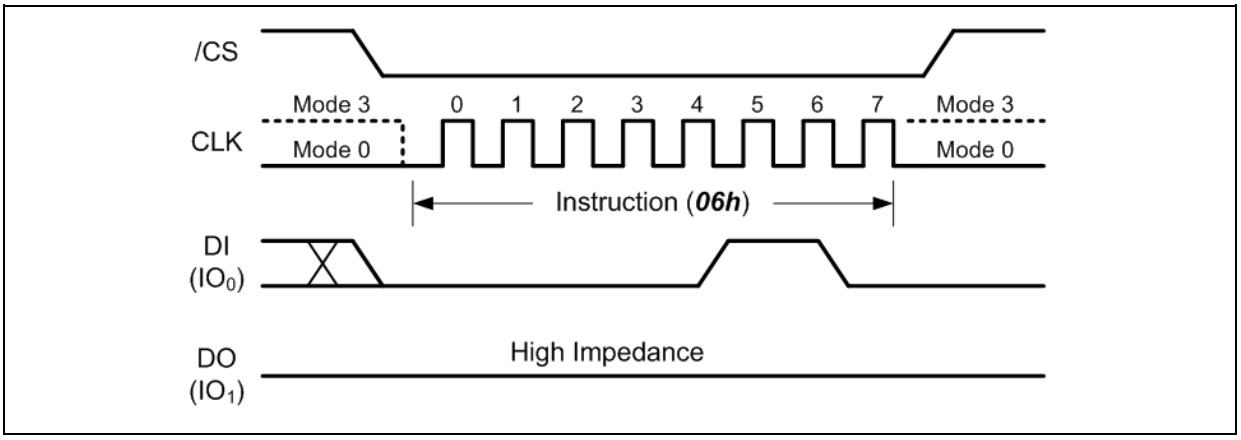


Figure 9. Write Enable Instruction

7.2.6 Write Disable (04h)

The Write Disable instruction (Figure 10) resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable instruction is entered by driving /CS low, shifting the instruction code “04h” into the DI pin and then driving /CS high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Page Program, Quad Page Program, Block Erase and Reset instructions.

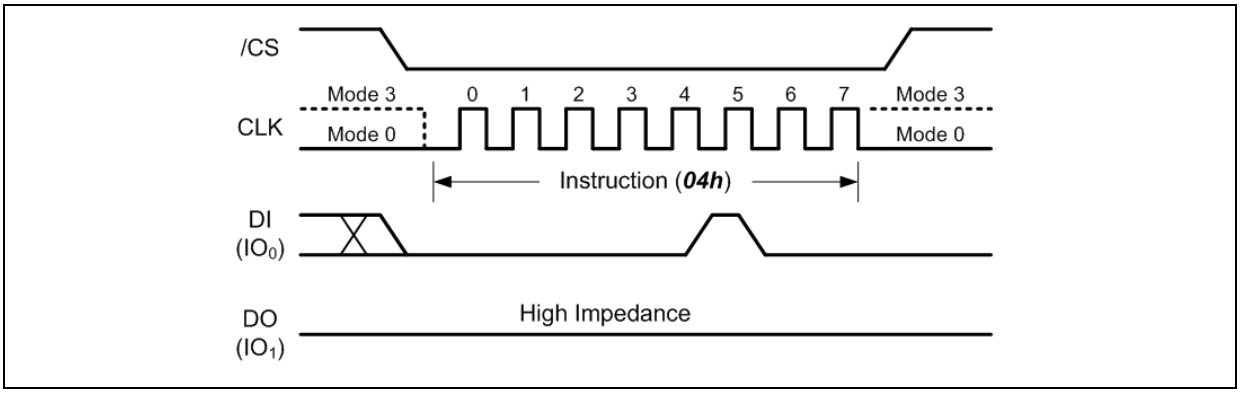


Figure 10. Write Disable Instruction

7.2.7 Bad Block Management (A1h)

Due to large NAND memory density size and the technology limitation, NAND memory devices are allowed to be shipped to the end customers with certain amount of “Bad Blocks” found in the factory testing. Up to 2% of the memory blocks can be marked as “Bad Blocks” upon shipment, which is a maximum of 20 blocks for W25N01GV. In order to identify these bad blocks, it is recommended to scan the entire memory array for bad block markers set in the factory. A “Bad Block Marker” is a non-FFh data byte stored at Byte 0 of Page 0 for each bad block. An additional marker is also stored in the first byte of the 64-Byte spare area.

W25N01GV offers a convenient method to manage the bad blocks typically found in NAND flash memory after extensive use. The “Bad Block Management” command is initiated by shifting the instruction code “A1h” into the DI pin and followed by the 16-bit “Logical Block Address” and 16-bit “Physical Block Address” as illustrated in Figure 11. The logical block address is the address for the “bad” block that will be replaced by the “good” block indicated by the physical block address.

Once a Bad Block Management command is successfully executed, the specified LBA-PBA link will be added to the internal Look Up Table (LUT). Up to 20 links can be established in the non-volatile LUT. If all 20 links have been written, the LUT-F bit in the Status Register will become a 1, and no more LBA-PBA links can be established. Therefore, prior to issuing the Bad Block Management command, the LUT-F bit value can be checked or a “Read BBM Look Up Table” command can be issued to confirm if spare links are still available in the LUT.

To guarantee a continuous read operation on the first 1,000 blocks, the manufacturer may have used some of the BBM LUT entrees. It is advisable for the user to scan all blocks and keep a table of all manufacturer bad blocks prior to first erase/program operation.

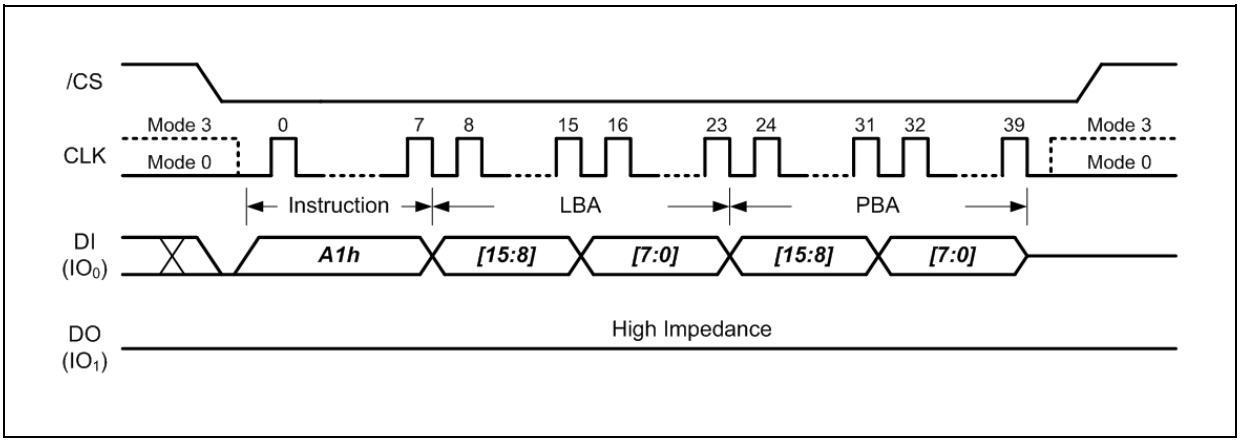


Figure 11. Bad Block Management Instruction

7.2.8 Read BBM Look Up Table (A5h)

The internal Look Up Table (LUT) consists of 20 Logical-Physical memory block links (from LBA0/PBA0 to LBA19/PBA19). The "Read BBM Look Up Table" command can be used to check the existing address links stored inside the LUT.

The "Read BBM Look Up Table" command is initiated by shifting the instruction code "A5h" into the DI pin and followed by 8-bit dummy clocks, at the falling edge of the 16th clocks, the device will start to output the 16-bit "Logical Block Address" and the 16-bit "Physical Block Address" as illustrated in Figure 12. All block address links will be output sequentially starting from the first link (LBA0 & PBA0) in the LUT. If there are available links that are unused, the output will contain all "00h" data.

The MSB bits LBA[15:14] of each link are used to indicate the status of the link.

LBA[15] (Enable)	LBA[14] (Invalid)	Descriptions
0	0	This link is available to use.
1	0	This link is enabled and it is a valid link.
1	1	This link was enabled, but it is not valid any more.
0	1	Not applicable.

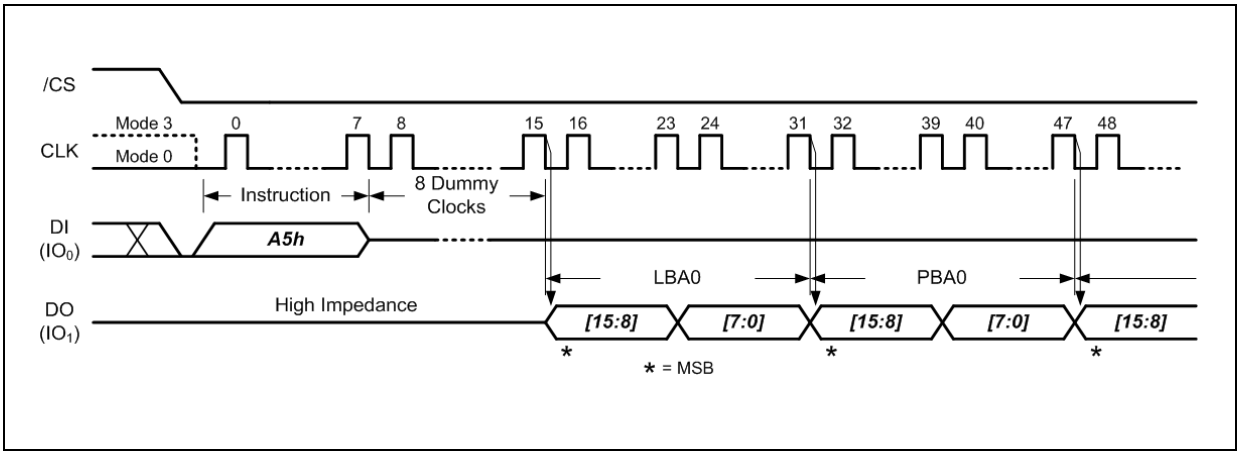


Figure 12. Read BBM Look Up Table Instruction

7.2.9 Last ECC Failure Page Address (A9h)

To better manage the data integrity, W25N01GV implements internal ECC correction for the entire memory array. When the ECC-E bit in the Status/Configuration Register is set to 1 (also power up default), the internal ECC algorithm is enabled for all Program and Read operations. During a “Program Execute” command for a specific page, the ECC algorithm will calculate the ECC information based on the data inside the 2K-Byte data buffer and write the ECC data into the extra 64-Byte ECC area in the same physical memory page.

During the Read operations, ECC information will be used to verify the data read out from the physical memory array and possible corrections can be made to limited amount of data bits that contain errors. The ECC Status Bits (ECC-1 & ECC-0) will also be set indicating the result of ECC calculation.

For the “Continuous Read Mode (BUF=0)” operation, multiple pages of main array data can be read out continuously by issuing a single read command. Upon finishing the read operation, the ECC status bits should be check to verify if there’s any ECC correction or un-correctable errors existed in the read out data. If ECC-1 & ECC-0 equal to (1, 0) or (1, 1), the previous read out data contain one or more pages that contain ECC un-correctable errors. The failure page address (or the last page address if it’s multiple pages) can be obtained by issuing the “Last ECC failure Page Address” command as illustrated in Figure 13. The 16-bit Page Address that contains un-correctable ECC errors will be presented on the DO pin following the instruction code “A9h” and 8-bit dummy clocks on the DI pin.

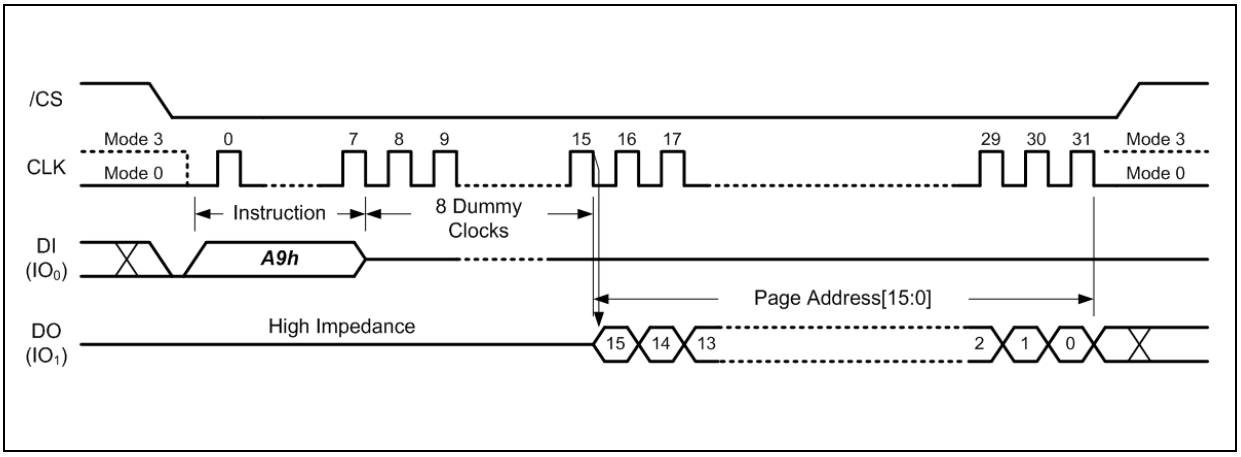


Figure 13. Last ECC Failure Page Address Instruction

7.2.10 128KB Block Erase (D8h)

The 128KB Block Erase instruction sets all memory within a specified block (64-Pages, 128K-Bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code "D8h" followed by 8-bit dummy clocks and the 16-bit page address. The Block Erase instruction sequence is shown in Figure 14.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After /CS is driven high, the self-timed Block Erase instruction will commence for a time duration of t_{BE} (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed block is protected by the Block Protect (TB, BP2, BP1, and BP0) bits.

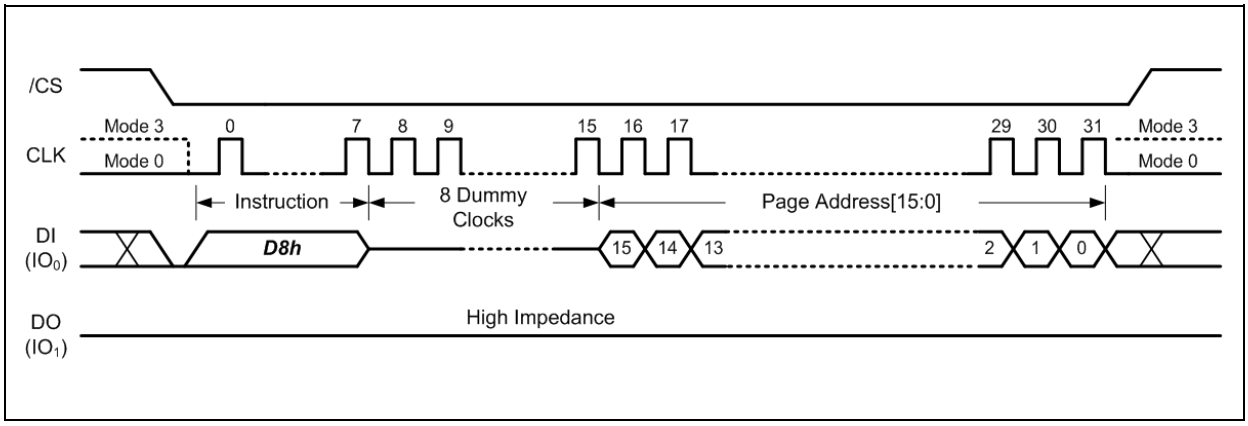


Figure 14. 128KB Block Erase Instruction

7.2.11 Load Program Data (02h) / Random Load Program Data (84h)

The Program operation allows from one byte to 2,112 bytes (a page) of data to be programmed at previously erased (FFh) memory locations. A Program operation involves two steps: 1. Load the program data into the Data Buffer. 2. Issue “Program Execute” command to transfer the data from Data Buffer to the specified memory page.

A Write Enable instruction must be executed before the device will accept the Load Program Data Instructions (Status Register bit WEL= 1). The “Load Program Data” or “Random Load Program Data” instruction is initiated by driving the /CS pin low then shifting the instruction code “02h” or “84h” followed by a 16-bit column address (only CA[11:0] is effective) and at least one byte of data into the DI pin. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. If the number of data bytes sent to the device exceeds the number of data bytes in the Data Buffer, the extra data will be ignored by the device. The Load Program Data instruction sequence is shown in Figure 15.

Both “Load Program Data” and “Random Load Program Data” instructions share the same command sequence. The difference is that “Load Program Data” instruction will reset the unused the data bytes in the Data Buffer to FFh value, while “Random Load Program Data” instruction will only update the data bytes that are specified by the command input sequence, the rest of the Data Buffer will remain unchanged.

If internal ECC algorithm is enabled, all 2,112 bytes of data will be accepted, but the bytes designated for ECC parity bits in the extra 64 bytes section will be overwritten by the ECC calculation. If the ECC-E bit is set to a 0 to disable the internal ECC, the extra 64 bytes section can be used for external ECC purpose or other usage.

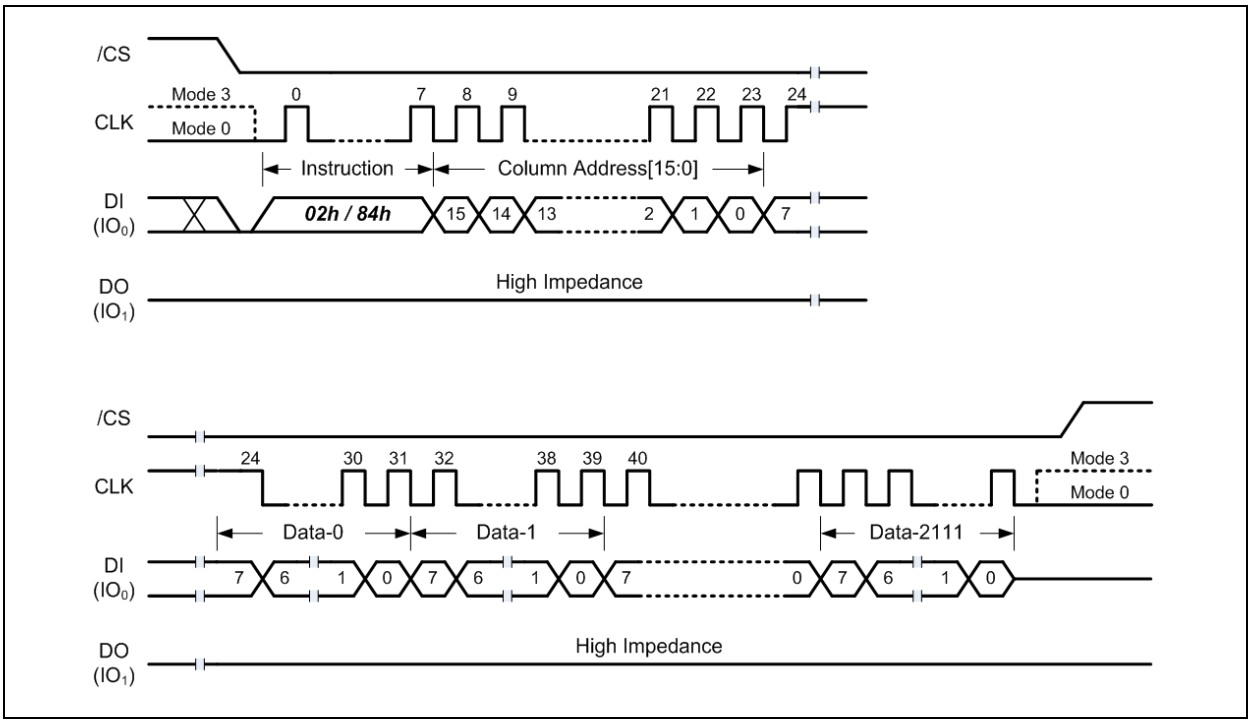


Figure 15. Load / Random Load Program Data Instruction

7.2.12 Quad Load Program Data (32h) / Quad Random Load Program Data (34h)

The “Quad Load Program Data” and “Quad Random Load Program Data” instructions are identical to the “Load Program Data” and “Random Load Program Data” in terms of operation sequence and functionality. The only difference is that “Quad Load” instructions will input the data bytes from all four IO pins instead of the single DI pin. This method will significantly shorten the data input time when a large amount of data needs to be loaded into the Data Buffer. The instruction sequence is illustrated in Figure 16.

Both “Quad Load Program Data” and “Quad Random Load Program Data” instructions share the same command sequence. The difference is that “Quad Load Program Data” instruction will reset the unused the data bytes in the Data Buffer to FFh value, while “Quad Random Load Program Data” instruction will only update the data bytes that are specified by the command input sequence, the rest of the Data Buffer will remain unchanged.

When WP-E bit in the Status Register is set to a 1, all Quad SPI instructions are disabled.

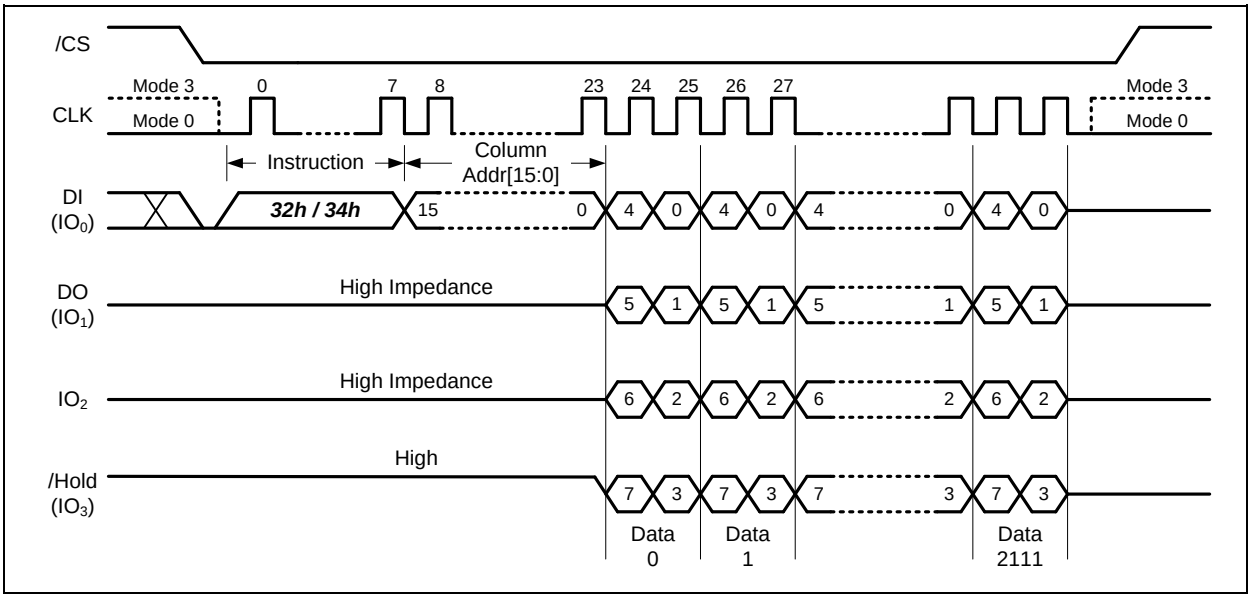


Figure 16. Quad Load / Quad Random Load Program Data Instruction

7.2.13 Program Execute (10h)

The Program Execute instruction is the second step of the Program operation. After the program data are loaded into the 2,112-Byte Data Buffer (or 2,048 bytes when ECC is enabled), the Program Execute instruction will program the Data Buffer content into the physical memory page that is specified in the instruction. The instruction is initiated by driving the /CS pin low then shifting the instruction code “10h” followed by 8-bit dummy clocks and the 16-bit Page Address into the DI pin as shown in Figure 17.

After /CS is driven high to complete the instruction cycle, the self-timed Program Execute instruction will commence for a time duration of tpp (See AC Characteristics). While the Program Execute cycle is in progress, the Read Status Register instruction may still be used for checking the status of the BUSY bit. The BUSY bit is a 1 during the Program Execute cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Program Execute cycle has finished, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Program Execute instruction will not be executed if the addressed page is protected by the Block Protect (TB, BP2, BP1, and BP0) bits.

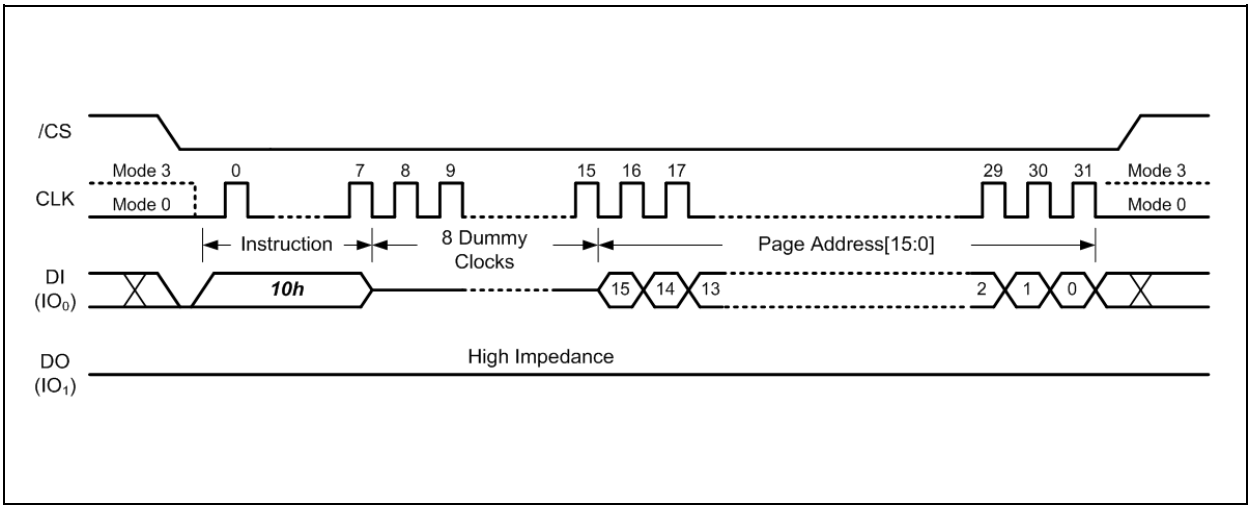


Figure 17. Program Execute Instruction

7.2.14 Page Data Read (13h)

The Page Data Read instruction will transfer the data of the specified memory page into the 2,112-Byte Data Buffer. The instruction is initiated by driving the /CS pin low then shifting the instruction code “13h” followed by 8-bit dummy clocks and the 16-bit Page Address into the DI pin as shown in Figure 18.

After /CS is driven high to complete the instruction cycle, the self-timed Read Page Data instruction will commence for a time duration of tRD (See AC Characteristics). While the Read Page Data cycle is in progress, the Read Status Register instruction may still be used for checking the status of the BUSY bit. The BUSY bit is a 1 during the Read Page Data cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again.

After the 2,112 bytes of page data are loaded into the Data Buffer, several Read instructions can be issued to access the Data Buffer and read out the data. Depending on the BUF bit setting in the Status Register, either “Buffer Read Mode” or “Continuous Read Mode” may be used to accomplish the read operations.

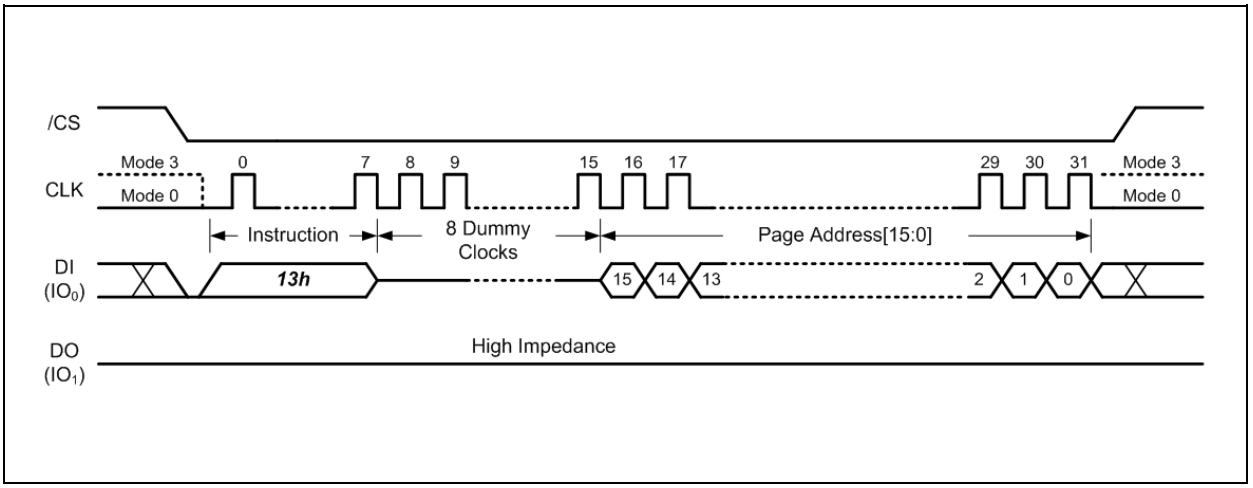


Figure 18. Page Data Read Instruction

7.2.15 Read Data (03h)

The Read Data instruction allows one or more data bytes to be sequentially read from the Data Buffer after executing the Read Page Data instruction. The Read Data instruction is initiated by driving the /CS pin low and then shifting the instruction code “03h” followed by the 16-bit Column Address and 8-bit dummy clocks or a 24-bit dummy clocks into the DI pin. After the address is received, the data byte of the addressed Data Buffer location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. The instruction is completed by driving /CS high.

The Read Data instruction sequence is shown in Figure 19a & 19b. When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bit Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state. When BUF=0, the device is in the Continuous Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of next memory page will be following and continues through the entire memory array. This allows using a single Read instruction to read out the entire memory array and is also compatible to Winbond’s SpiFlash NOR flash memory command sequence.

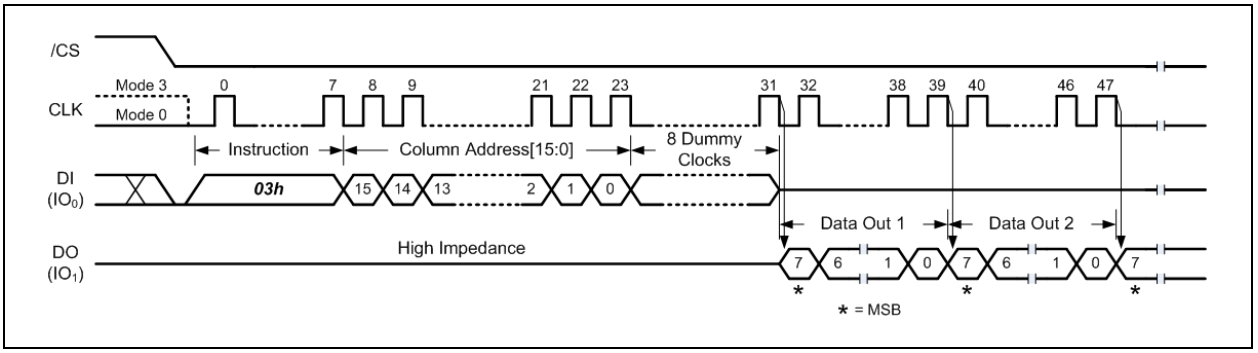


Figure 19a. Read Data Instruction (Buffer Read Mode, BUF=1)

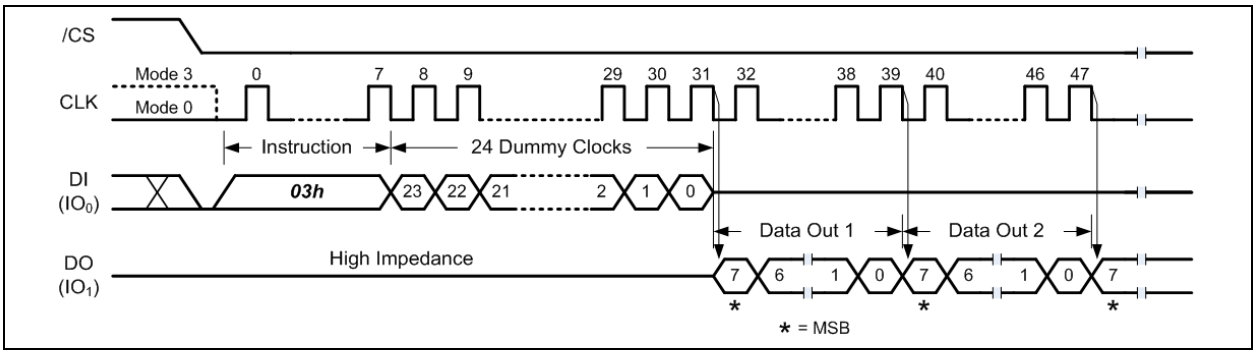


Figure 19b. Read Data Instruction (Continuous Read Mode, BUF=0)

7.2.16 Fast Read (0Bh)

The Fast Read instruction allows one or more data bytes to be sequentially read from the Data Buffer after executing the Read Page Data instruction. The Fast Read instruction is initiated by driving the /CS pin low and then shifting the instruction code “0Bh” followed by the 16-bit Column Address and 8-bit dummy clocks or a 32-bit dummy clocks into the DI pin. After the address is received, the data byte of the addressed Data Buffer location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. The instruction is completed by driving /CS high.

The Fast Read instruction sequence is shown in Figure 20a & 20b. When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bit Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state. When BUF=0, the device is in the Continuous Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of next memory page will be following and continues through the entire memory array. This allows using a single Read instruction to read out the entire memory array and is also compatible to Winbond’s SpiFlash NOR flash memory command sequence.

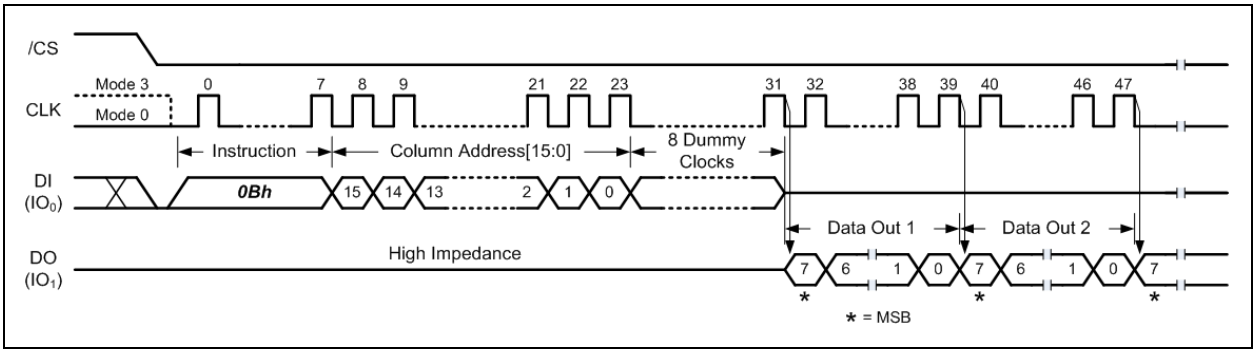


Figure 20a. Fast Read Instruction (Buffer Read Mode, BUF=1)

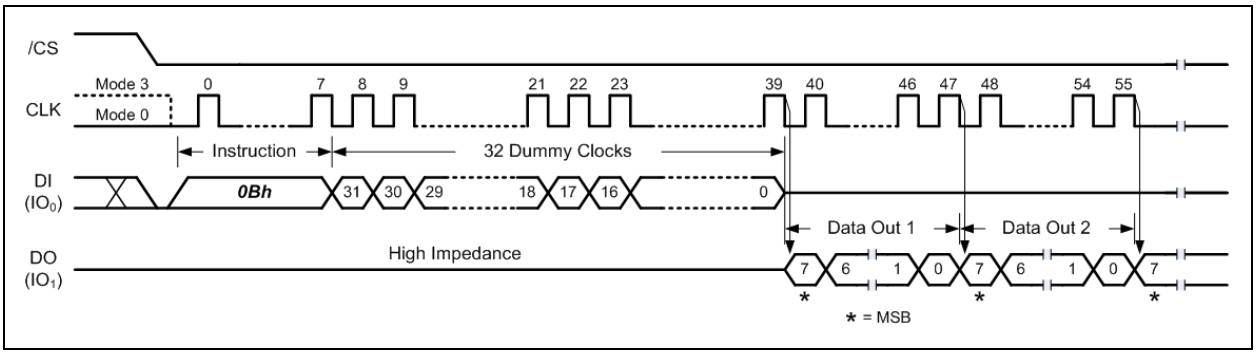


Figure 20b. Fast Read Instruction (Continuous Read Mode, BUF=0)

7.2.17 Fast Read with 4-Byte Address (0Ch)

The Fast Read instruction allows one or more data bytes to be sequentially read from the Data Buffer after executing the Read Page Data instruction. The Fast Read instruction is initiated by driving the /CS pin low and then shifting the instruction code “0Ch” followed by the 16-bit Column Address and 24-bit dummy clocks (when BUF=1) or a 40-bit dummy clocks (when BUF=0) into the DI pin. After the address is received, the data byte of the addressed Data Buffer location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. The instruction is completed by driving /CS high.

The Fast Read instruction sequence is shown in Figure 21a & 21b. When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bit Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state. When BUF=0, the device is in the Continuous Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of next memory page will be following and continues through the entire memory array. This allows using a single Read instruction to read out the entire memory array and is also compatible to Winbond’s SpiFlash NOR flash memory command sequence.

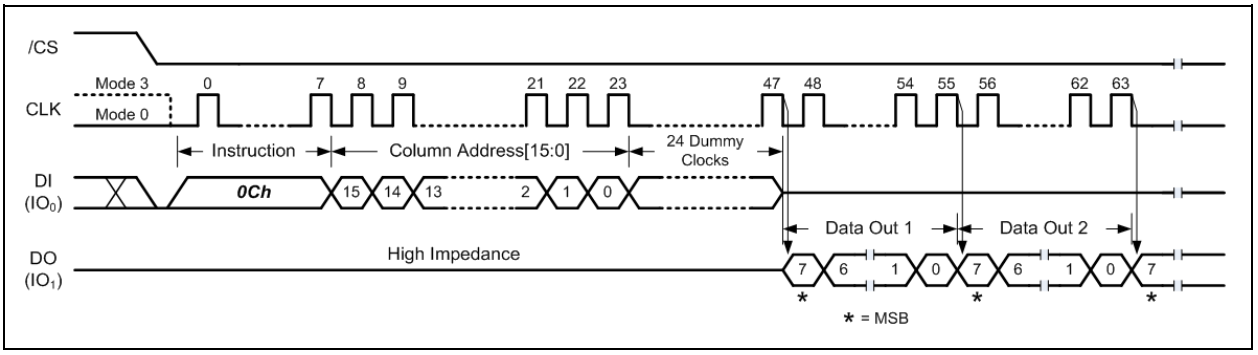


Figure 21a. Fast Read with 4-Byte Address Instruction (Buffer Read Mode, BUF=1)

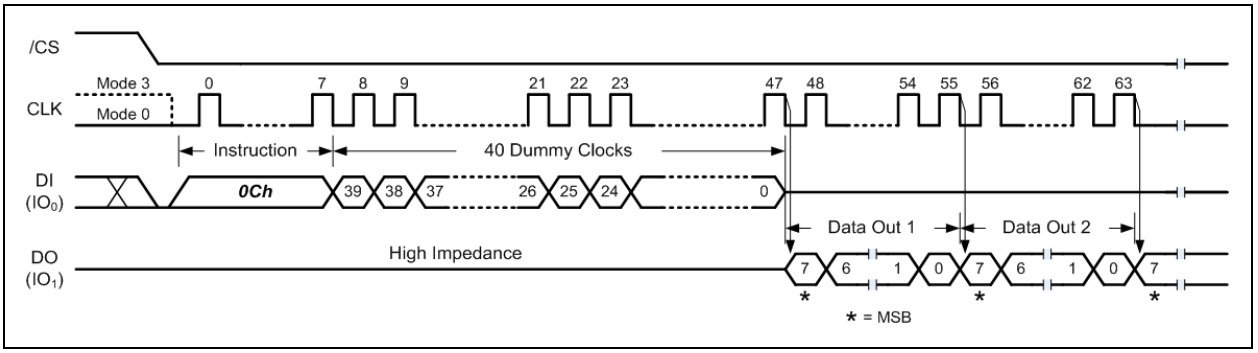


Figure 21b. Fast Read with 4-Byte Address Instruction (Continuous Read Mode, BUF=0)

7.2.18 Fast Read Dual Output (3Bh)

The Fast Read Dual Output (3Bh) instruction is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins; IO_0 and IO_1. This allows data to be transferred at twice the rate of standard SPI devices.

The Fast Read Dual Output instruction sequence is shown in Figure 22a & 22b. When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bit Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state. When BUF=0, the device is in the Continuous Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of next memory page will be following and continues through the entire memory array. This allows using a single Read instruction to read out the entire memory array and is also compatible to Winbond's SpiFlash NOR flash memory command sequence.

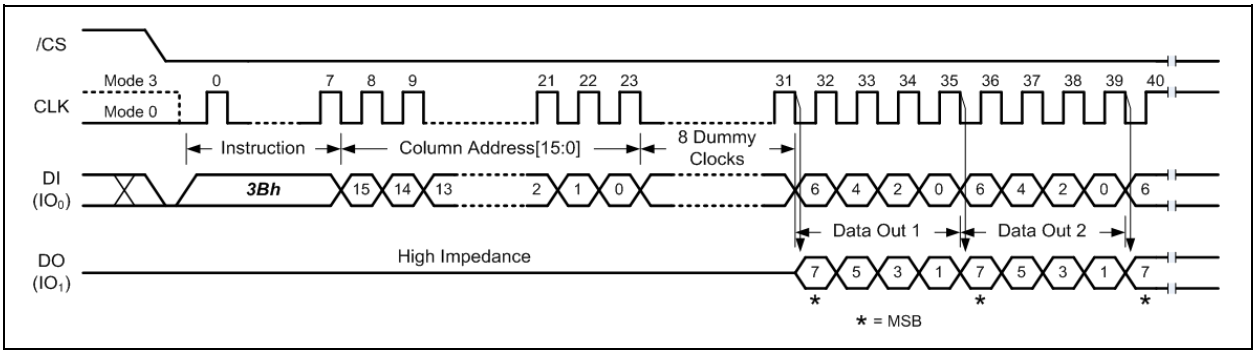


Figure 22a. Fast Read Dual Output Instruction (Buffer Read Mode, BUF=1)

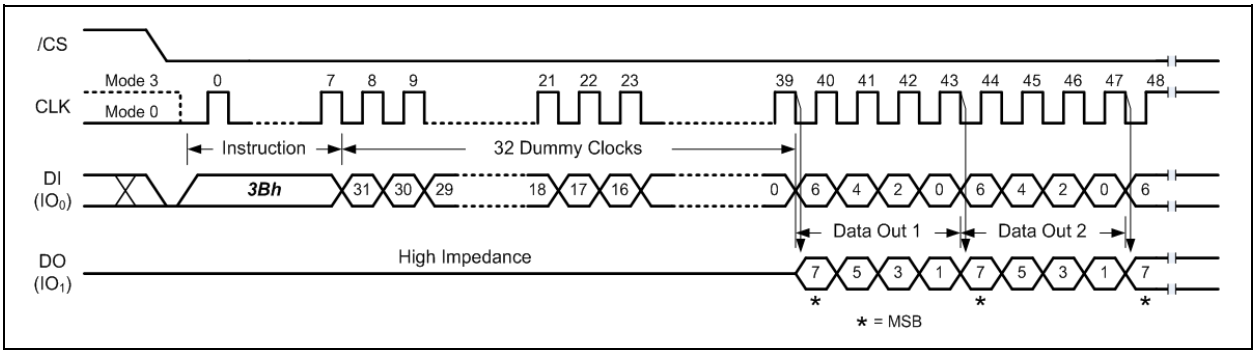


Figure 22b. Fast Read Dual Output Instruction (Continuous Read Mode, BUF=0)

7.2.19 Fast Read Dual Output with 4-Byte Address (3Ch)

The Fast Read Dual Output (3Ch) instruction is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins; IO_0 and IO_1. This allows data to be transferred at twice the rate of standard SPI devices.

The Fast Read Dual Output instruction sequence is shown in Figure 23a & 23b. When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bit Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state. When BUF=0, the device is in the Continuous Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of next memory page will be following and continues through the entire memory array. This allows using a single Read instruction to read out the entire memory array and is also compatible to Winbond's SpiFlash NOR flash memory command sequence.

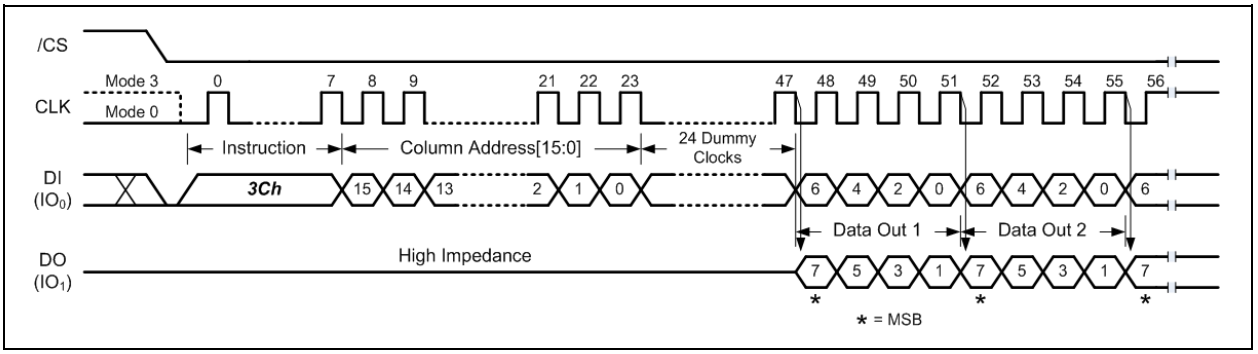


Figure 23a. Fast Read Dual Output with 4-Byte Address Instruction (Buffer Read Mode, BUF=1)

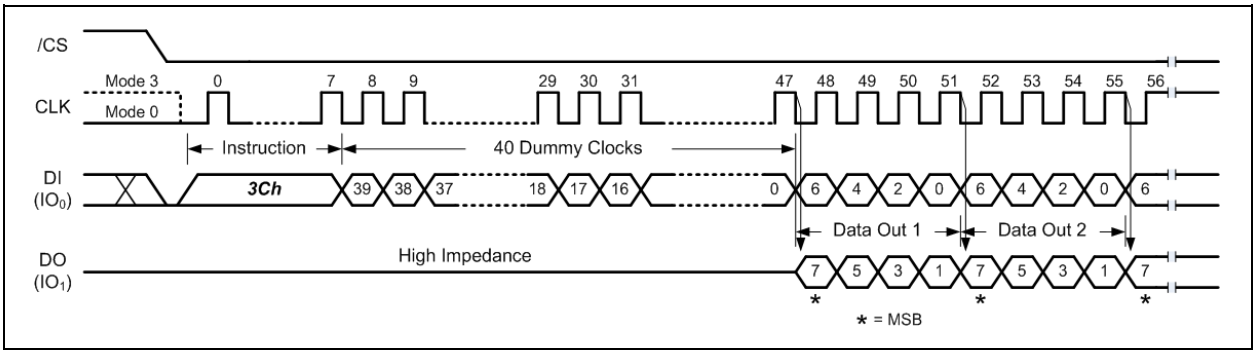


Figure 23b. Fast Read Dual Output with 4-Byte Address Instruction (Continuous Read Mode, BUF=0)

7.2.20 Fast Read Quad Output (6Bh)

The Fast Read Quad Output (6Bh) instruction is similar to the Fast Read Dual Output (3Bh) instruction except that data is output on four pins, IO_0, IO_1, IO_2, and IO_3. The Fast Read Quad Output Instruction allows data to be transferred at four times the rate of standard SPI devices.

The Fast Read Quad Output instruction sequence is shown in Figure 24a & 24b. When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bit Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state. When BUF=0, the device is in the Continuous Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of next memory page will be following and continues through the entire memory array. This allows using a single Read instruction to read out the entire memory array and is also compatible to Winbond's SpiFlash NOR flash memory command sequence.

When WP-E bit in the Status Register is set to a 1, this instruction is disabled.

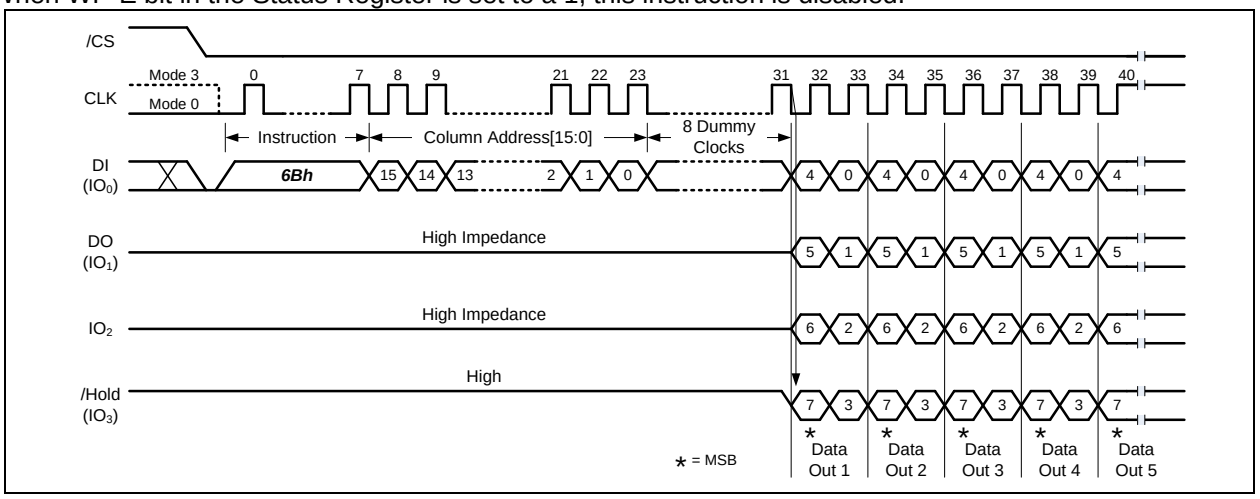


Figure 24a. Fast Read Quad Output Instruction (Buffer Read Mode, BUF=1)

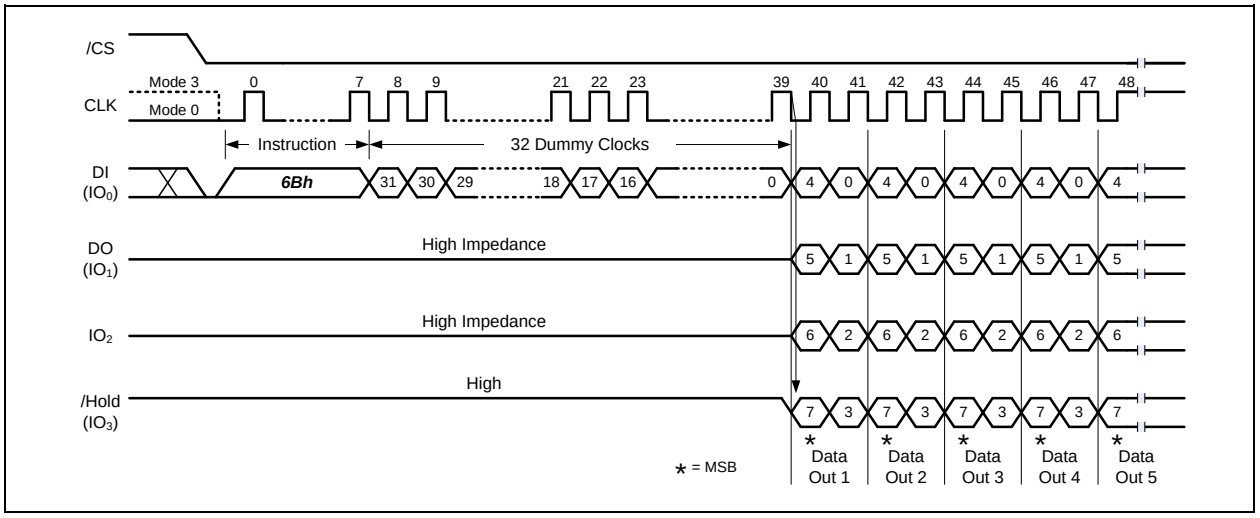


Figure 24b. Fast Read Quad Output Instruction (Continuous Read Mode, BUF=0)

7.2.21 Fast Read Quad Output with 4-Byte Address (6Ch)

The Fast Read Quad Output (6Ch) instruction is similar to the Fast Read Dual Output (3Bh) instruction except that data is output on four pins, IO_0, IO_1, IO_2, and IO_3. The Fast Read Quad Output Instruction allows data to be transferred at four times the rate of standard SPI devices.

The Fast Read Quad Output instruction sequence is shown in Figure 25a & 25b. When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bit Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state. When BUF=0, the device is in the Continuous Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of next memory page will be following and continues through the entire memory array. This allows using a single Read instruction to read out the entire memory array and is also compatible to Winbond's SpiFlash NOR flash memory command sequence.

When WP-E bit in the Status Register is set to a 1, this instruction is disabled.

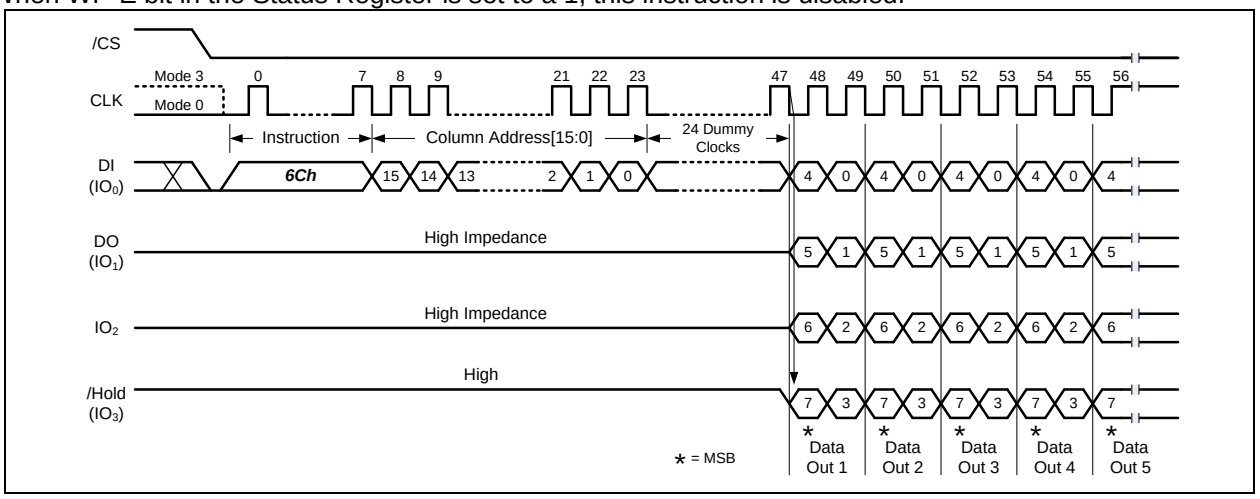


Figure 25a. Fast Read Quad Output with 4-Byte Address Instruction (Buffer Read Mode, BUF=1)

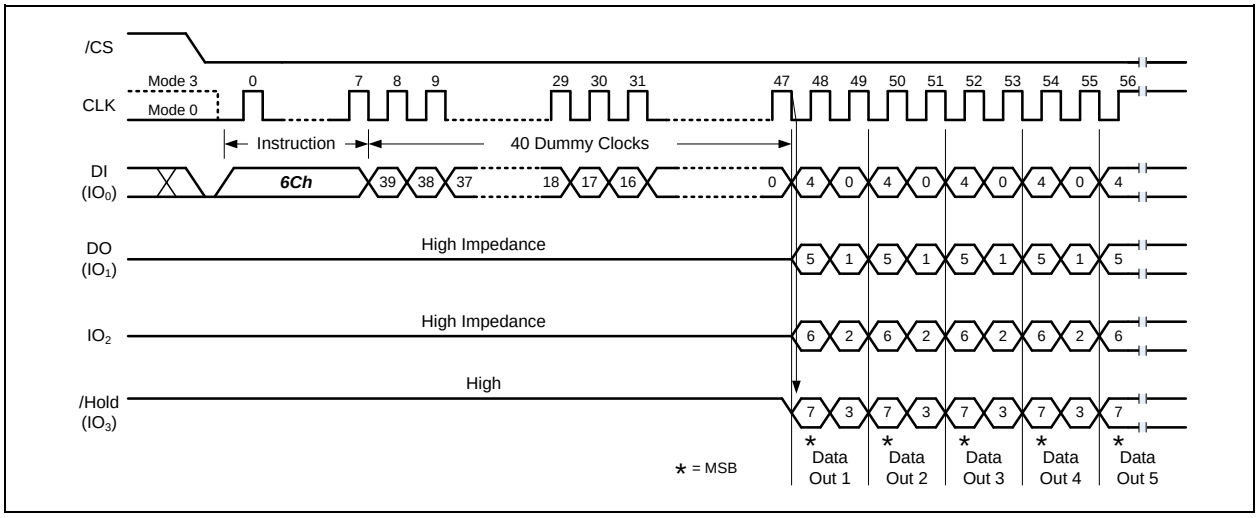


Figure 25b. Fast Read Quad Output with 4-Byte Address Instruction (Continuous Read Mode, BUF=0)

7.2.22 Fast Read Dual I/O (BBh)

The Fast Read Dual I/O (BBh) instruction allows for improved random access while maintaining two IO pins, IO_0 and IO_1. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the Column Address or the dummy clocks two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

The Fast Read Quad Output instruction sequence is shown in Figure 26a & 26b. When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bit Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state. When BUF=0, the device is in the Continuous Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of next memory page will be following and continues through the entire memory array. This allows using a single Read instruction to read out the entire memory array and is also compatible to Winbond's SpiFlash NOR flash memory command sequence.

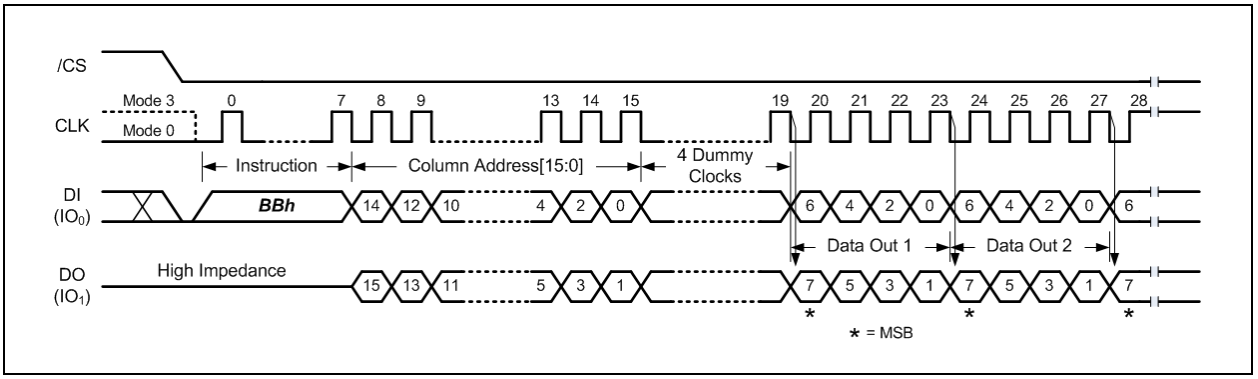


Figure 26a. Fast Read Dual I/O Instruction (Buffer Read Mode, BUF=1)

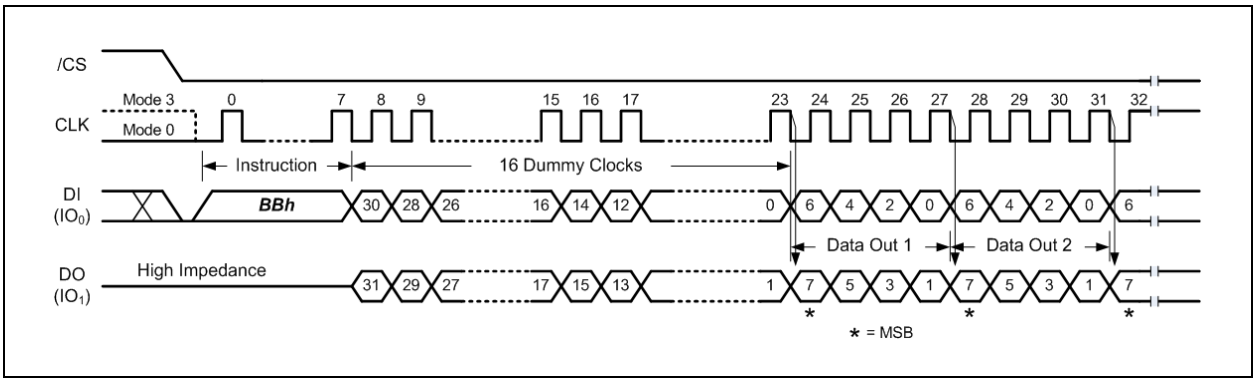


Figure 26b. Fast Read Dual I/O Instruction (Continuous Read Mode, BUF=0)

7.2.23 Fast Read Dual I/O with 4-Byte Address (BCh)

The Fast Read Dual I/O (BCh) instruction allows for improved random access while maintaining two IO pins, IO_0 and IO_1. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the Column Address or the dummy clocks two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

The Fast Read Quad Output instruction sequence is shown in Figure 27a & 27b. When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bit Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state. When BUF=0, the device is in the Continuous Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of next memory page will be following and continues through the entire memory array. This allows using a single Read instruction to read out the entire memory array and is also compatible to Winbond's SpiFlash NOR flash memory command sequence.

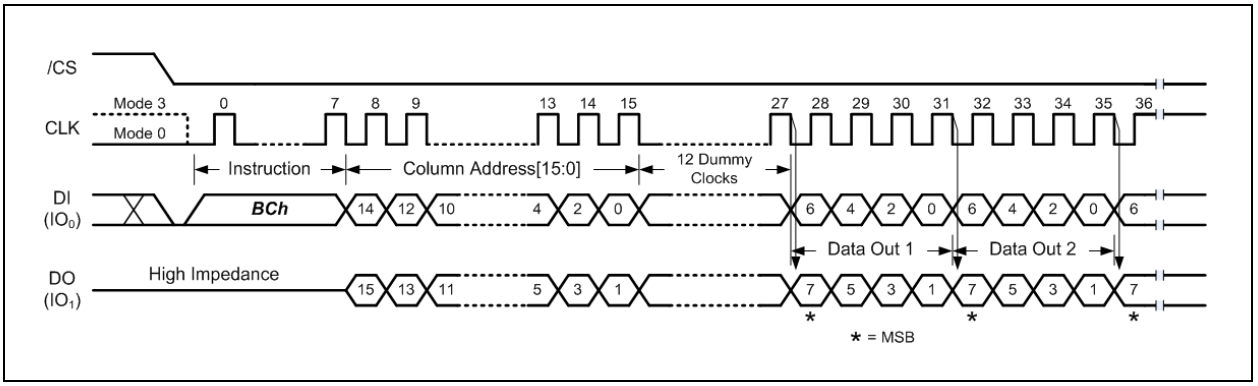


Figure 27a. Fast Read Dual I/O with 4-Byte Address Instruction (Buffer Read Mode, BUF=1)

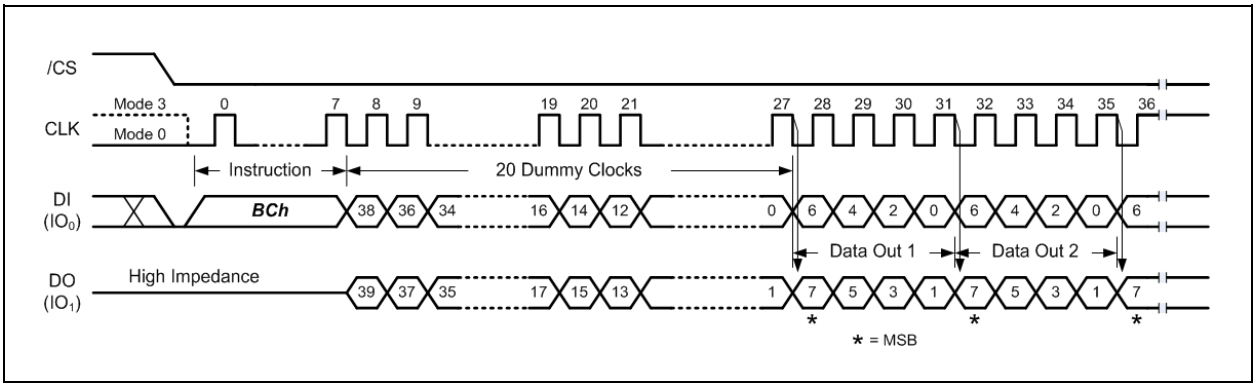


Figure 27b. Fast Read Dual I/O with 4-Byte Address Instruction (Continuous Read Mode, BUF=0)

7.2.24 Fast Read Quad I/O (EBh)

The Fast Read Quad I/O (EBh) instruction is similar to the Fast Read Dual I/O (BBh) instruction except that address and data bits are input and output through four pins IO_0, IO_1, IO_2 and IO_3 prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI.

The Fast Read Quad Output instruction sequence is shown in Figure 28a & 28b. When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bit Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state. When BUF=0, the device is in the Continuous Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of next memory page will be following and continues through the entire memory array. This allows using a single Read instruction to read out the entire memory array and is also compatible to Winbond's SpiFlash NOR flash memory command sequence.

When WP-E bit in the Status Register is set to a 1, this instruction is disabled.

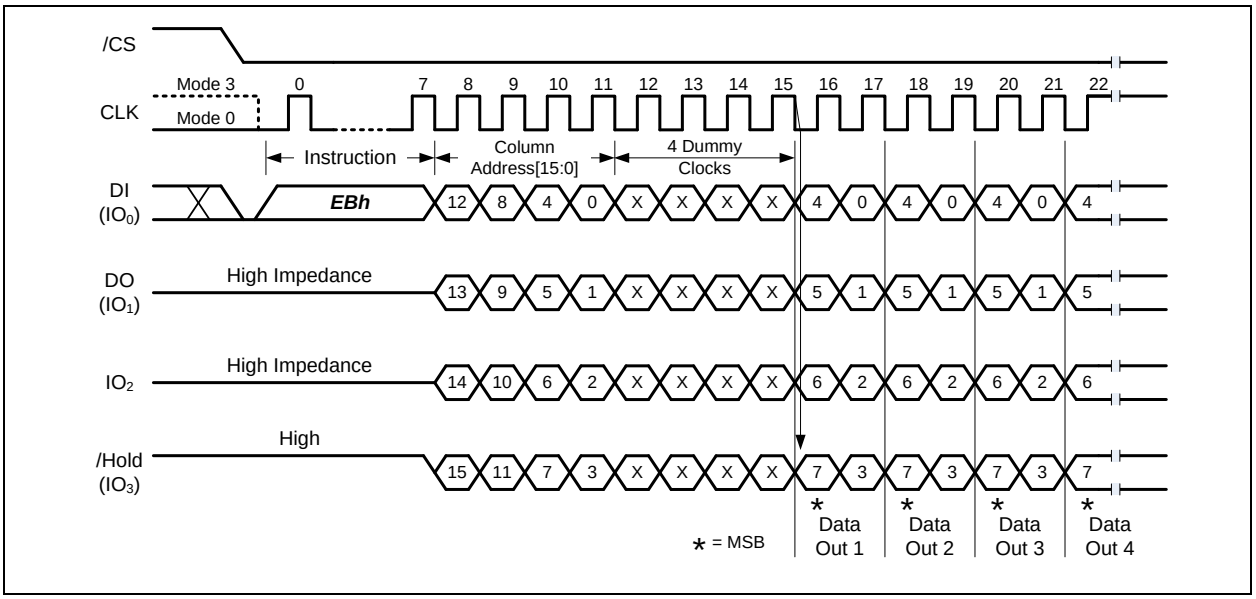


Figure 28a. Fast Read Quad I/O Instruction (Buffer Read Mode, BUF=1)

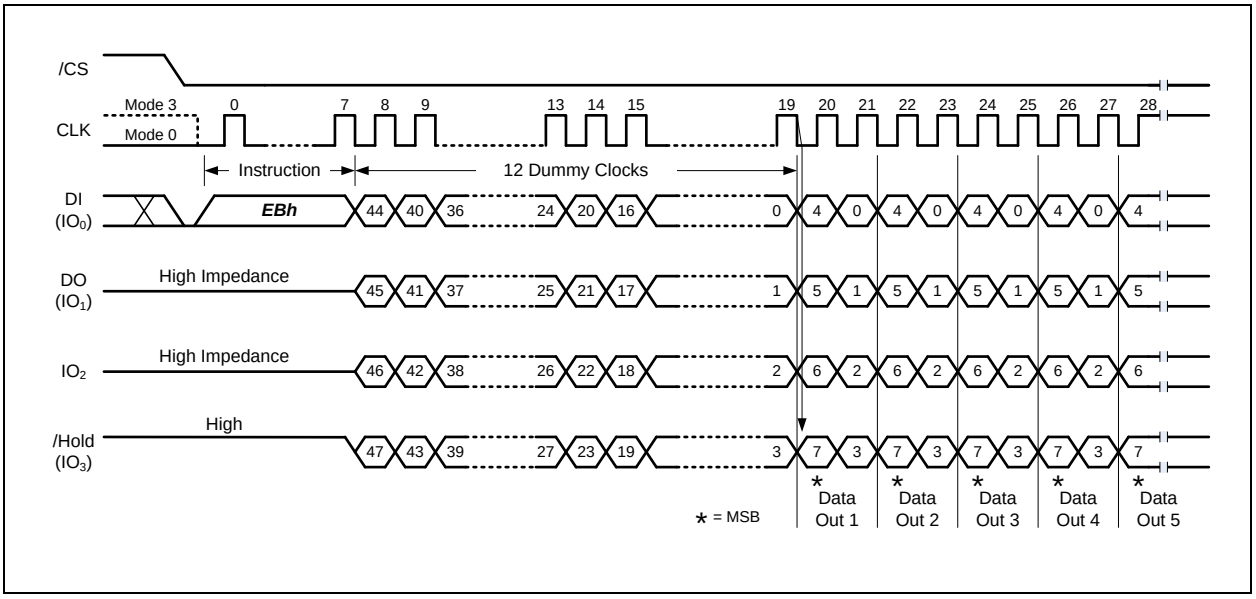


Figure 28b. Fast Read Quad I/O Instruction (Continuous Read Mode, BUF=0)

7.2.25 Fast Read Quad I/O with 4-Byte Address (ECh)

The Fast Read Quad I/O (ECh) instruction is similar to the Fast Read Dual I/O (BBh) instruction except that address and data bits are input and output through four pins IO_0, IO_1, IO_2 and IO_3 prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI.

The Fast Read Quad Output instruction sequence is shown in Figure 29a & 29b. When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bit Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state. When BUF=0, the device is in the Continuous Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of next memory page will be following and continues through the entire memory array. This allows using a single Read instruction to read out the entire memory array and is also compatible to Winbond's SpiFlash NOR flash memory command sequence.

When WP-E bit in the Status Register is set to a 1, this instruction is disabled.

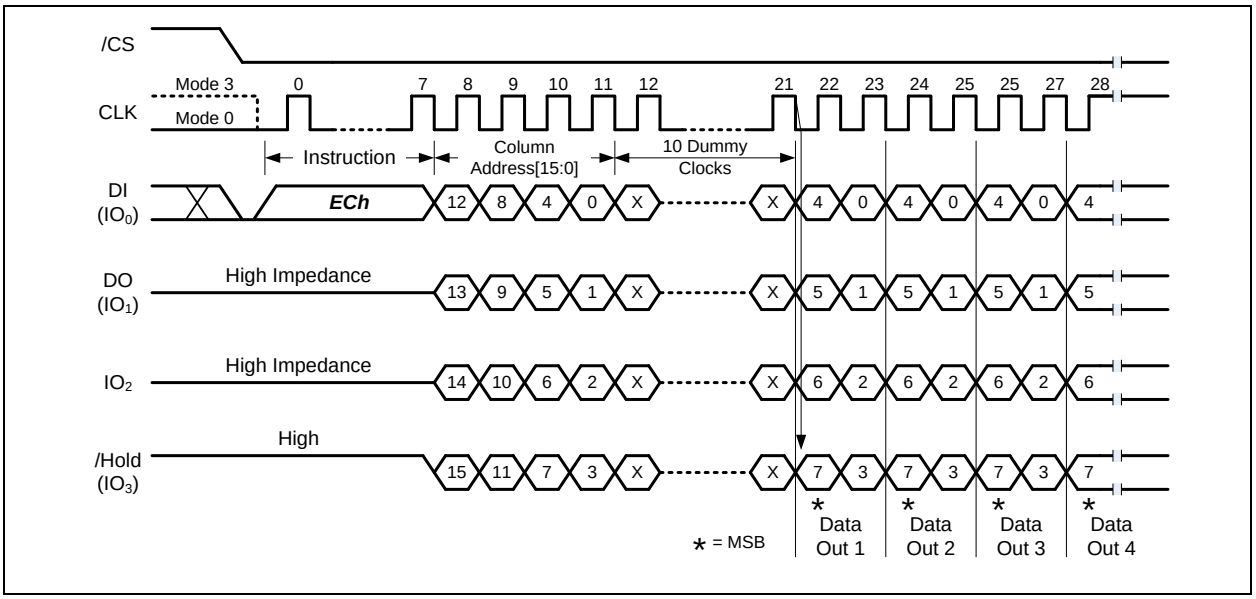


Figure 29a. Fast Read Quad I/O with 4-Byte Address Instruction (Buffer Read Mode, BUF=1)

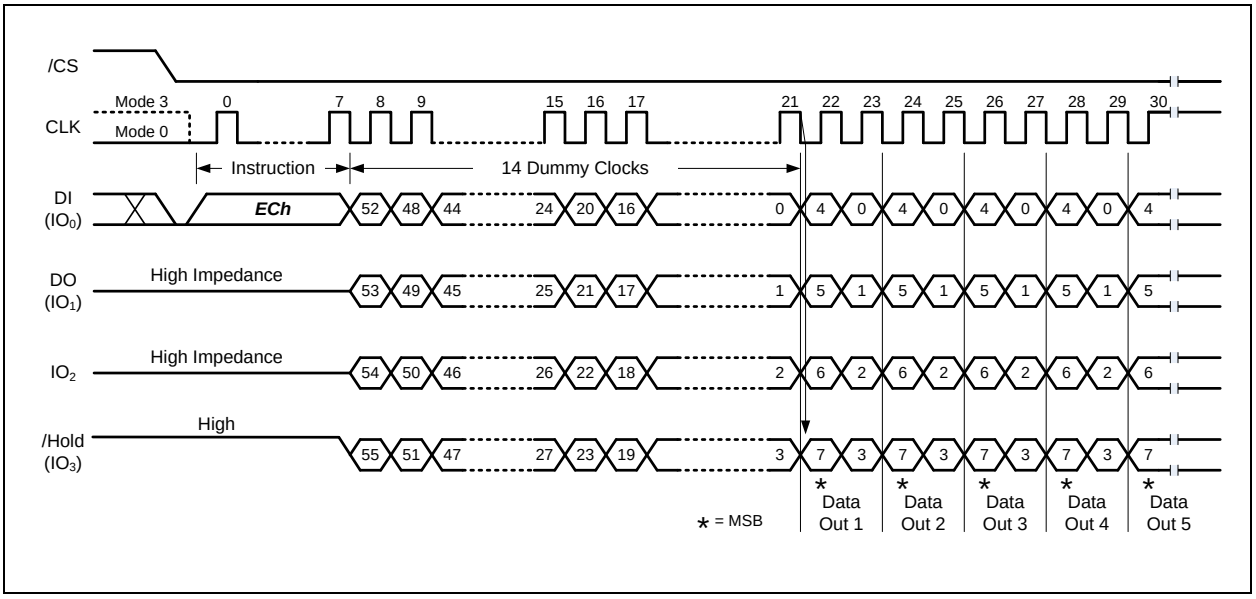


Figure 29b. Fast Read Quad I/O with 4-Byte Address Instruction (Continuous Read Mode, BUF=0)

7.2.26 Accessing Unique ID / Parameter / OTP Pages (OTP-E=1)

In addition to the main memory array, the W25N01GV is also equipped with one Unique ID Page, one Parameter Page, and ten OTP Pages.

Page Address	Page Name	Descriptions	Data Length
00h	Unique ID Page	Factory programmed, Read Only	32-Byte x 16
01h	Parameter Page	Factory programmed, Read Only	256-Byte x 3
02h	OTP Page [0]	Program Only, OTP lockable	2,112-Byte
…	OTP Pages [1:8]	Program Only, OTP lockable	2,112-Byte
0Bh	OTP Page [9]	Program Only, OTP lockable	2,112-Byte

To access these additional data pages, the OTP-E bit in Status Register-2 must be set to “1” first. Then, Read operations can be performed on Unique ID and Parameter Pages, Read and Program operations can be performed on the OTP pages if it’s not already locked. To return to the main memory array operation, OTP-E bit needs to be to set to 0.

Read Operations

A “Page Data Read” command must be issued followed by a specific page address shown in the table above to load the page data into the main Data Buffer. After the device finishes the data loading (BUSY=0), all Read commands may be used to read the Data Buffer starting from any specified Column Address. Please note all Read commands must now follow the “Buffer Read Mode” command structure (CA[15:0], number of dummy clocks) regardless the previous BUF bit setting. ECC can also be enabled for the OTP page read operations to ensure the data integrity.

Program and OTP Lock Operations

OTP pages provide the additional space (2K-Byte x 10) to store important data or security information that can be locked to prevent further modification in the field. These OTP pages are in an erased state set in the factory, and can only be programmed (change data from “1” to “0”) until being locked by OTP-L bit in the Configuration/Status Register-2. OTP-E must be first set to “1” to enable the access to these OTP pages, then the program data must be loaded into the main Data Buffer using any “Program Data Load” commands. The “Program Execute” command followed by a specific OTP Page Address is used to initiate the data transfer from the Data Buffer to the OTP page. When ECC is enabled, ECC calculation will be performed during “Program Execute”, and the ECC information will be stored into the 64-Byte spare area.

Once the OTP pages are correctly programmed, OTP-L bit can be used to permanently lock these pages so that no further modification is possible. While still in the “OTP Access Mode” (OTP-E=1), user needs to set OTP-L bit in the Configuration/Status Register-2 to “1”, and issue a “Program Execute” command(Page address is “don’t care”). After the device finishes the OTP lock setting (BUSY=0), the user can set OTP-E to “0” to return to the main memory array operation.

SR1-L OTP Lock Operation

The Protection/Status Register-1 contains protection bits that can be set to protect either a portion or the entire memory array from being Programmed/Erased or set the device to either Software Write Protection (WP-E=0) or Hardware Write Protection (WP-E=1). Once the BP[3:0], TB, WP-E bits are set correctly, SRP1 and SRP0 should also be set to “1”s as well to allow SR1-L bit being set to “1” to permanently lock the protection settings in the Status Register-1 (SR1). Similar to the OTP-L setting procedure above, in order to set SR1-L lock bit, the device must enter the “OTP Access Mode” (OTP-E=1) first, and SR1-L bit should be set to “1” prior to the “Program Execute” command (Page address is “don’t care”). Once SR1-L is set to “1” (BUSY=0), the user can set OTP-E to “0” to return to the main memory array operation.

7.2.27 Parameter Page Data Definitions

The Parameter Page contains 3 identical copies of the 256-Byte Parameter Data. The table below lists all the key data byte locations. All other unspecified byte locations have 00h data as default.

Byte Number	Descriptions	Values
0~3	Parameter page signature	4Fh, 4Eh, 46h, 49h
4~5	Revision number	00h, 00h
6~7	Feature supported	00h, 00h
8~9	Optional command supported	02h, 00h
10~31	Reserved	All 00h
32~43	Device manufacturer	57h, 49h, 4Eh, 42h, 4Fh, 4Eh, 44h, 20h, 20h, 20h, 20h, 20h
44~63	Device model	57h, 32h, 35h, 4Eh, 30h, 31h, 47h, 56h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
64	JEDEC manufacturer ID	EFh
65~66	Date code	00h, 00h
67~79	Reserved	All 00h
80~83	Number of data bytes per page	00h, 08h, 00h, 00h
84~85	Number of spare bytes per page	40h, 00h
86~91	Reserved	All 00h
92~95	Number of pages per block	40h, 00h, 00h, 00h
96~99	Number of blocks per logical unit	00h, 04h, 00h, 00h
100	Number of logical units	01h
101	Number of address bytes	00h
102	Number of bits per cell	01h
103~104	Bad blocks maximum per unit	14h, 00h
105~106	Block endurance	01h, 06h
107	Guaranteed valid blocks at beginning of target	01h
108~109	Block endurance for guaranteed valid blocks	00h, 00h
110	Number of programs per page	04h
111	Reserved	00h
112	Number of ECC bits	00h
113	Number of plane address bits	00h
114	Multi-plane operation attributes	00h
115~127	Reserved	All 00h
128	I/O pin capacitance, maximum	08h
129~132	Reserved	All 00h
133~134	Maximum page program time (us)	BCh, 02h
135~136	Maximum block erase time (us)	10h, 27h
137~138	Maximum page read time (us)	32h, 00h
139~163	Reserved	All 00h
164~165	Vendor specific revision number	00h, 00h
166~253	Vendor specific	All 00h
254~255	Integrity CRC	Set at test
256~511	Value of bytes 0~255	
512~767	Value of bytes 0~255	
768+	Reserved	

8. ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings (1)

PARAMETERS	SYMBOL	CONDITIONS	RANGE	UNIT
Supply Voltage	VCC		–0.6 to +4.6	V
Voltage Applied to Any Pin	VIO	Relative to Ground	–0.6 to VCC+0.4	V
Transient Voltage on any Pin	VIOT	<20nS Transient Relative to Ground	–2.0V to VCC+2.0V	V
Short Circuit Output Current, IOs			5	mA
Storage Temperature	TSTG		–65 to +150	°C
Lead Temperature	TLEAD		See Note (2)	°C
Electrostatic Discharge Voltage	VESD	Human Body Model(3)	–2000 to +2000	V

Notes:

1. This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.
2. Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.
3. JEDEC Standard JESD22-A114A (C1=100pF, R1=1500 ohms, R2=500 ohms).

8.2 Operating Ranges

PARAMETER	SYMBOL	CONDITIONS	SPEC		UNIT
			MIN	MAX	
Supply Voltage	VCC		2.7	3.6	V
Ambient Temperature, Operating	TA	Industrial	–40	+85	°C

8.3 Power-up Power-down Timing Requirements

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
VCC (min) to /CS Low	t_{VSL}(1)	50	500	µs
Time Delay Before Write Instruction	t_{PUW}(1)	5		ms
Write Inhibit Threshold Voltage	V_{WI}(1)	1.0	2.0	V

Note:

1. These parameters are characterized only.

8.3.1 Power-up Timing and Voltage Levels

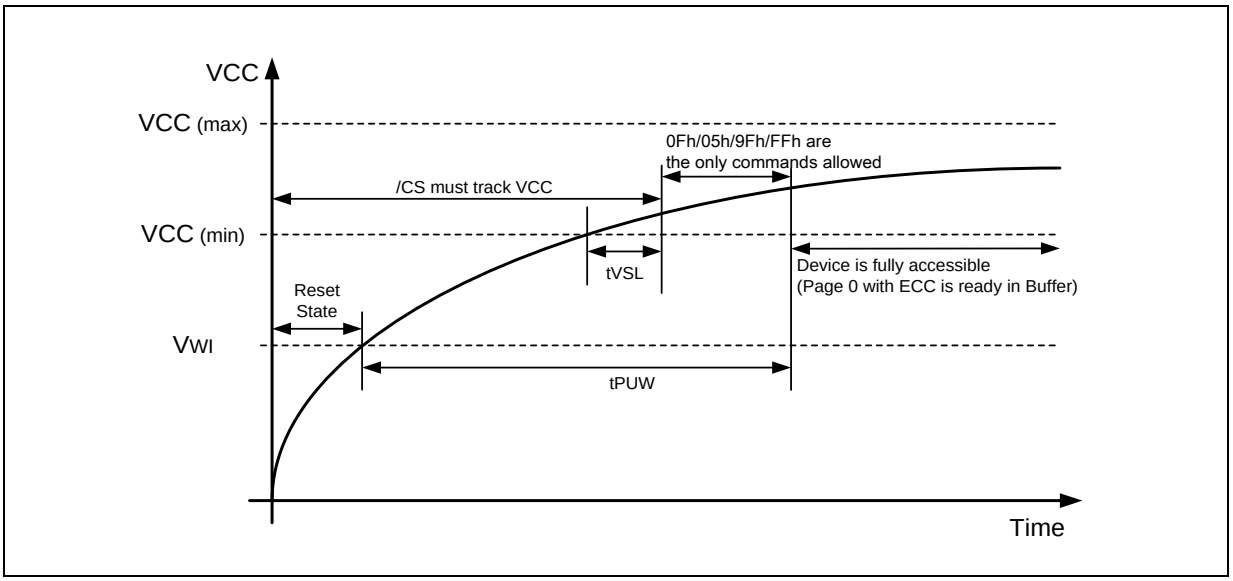


Figure 30a. Power-up Timing and Voltage Levels

8.3.2 Power-up, Power-Down Requirement

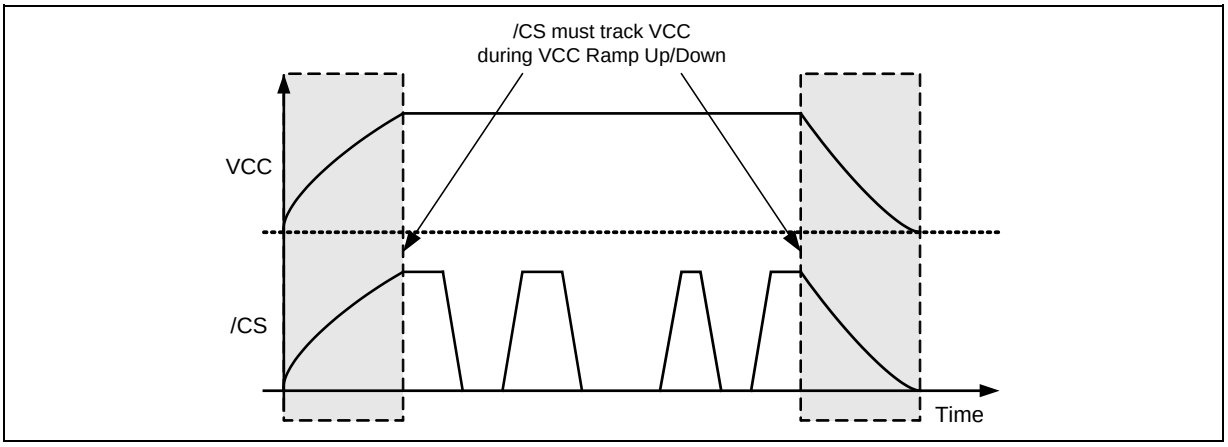


Figure 30b. Power-up, Power-Down Requirement

8.4 DC Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	
Input Capacitance	C_{IN}(1)	V_{IN} = 0V(1)			6	pF
Output Capacitance	Cout(1)	V_{OUT} = 0V(1)			8	pF
Input Leakage	I_{LI}				±2	µA
I/O Leakage	I_{LO}				±2	µA
Standby Current	I_{CC1}	/CS = VCC, VIN = GND or VCC		10	50	µA
Read Current	I_{CC2}	C = 0.1 VCC / 0.9 VCC DO = Open		25	35	mA
Current Page Program	I_{CC3}	/CS = VCC		25	35	mA
Current Block Erase	I_{CC4}	/CS = VCC		25	35	mA
Input Low Voltage	V_{IL}				VCC x 0.3	V
Input High Voltage	V_{IH}		VCC x 0.7			V
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA			0.4	V
Output High Voltage	V_{OH}	I_{OH} = –400 µA	2.4			V

Notes:

1. Tested on sample basis and specified through design and characterization data. TA = 25° C, VCC = 3.0V.

8.5 AC Measurement Conditions

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
Load Capacitance	C_L		30	pF
Input Rise and Fall Times	T_R, T_F		5	ns
Input Pulse Voltages	V_{IN}	0.1 VCC to 0.9 VCC		V
Input Timing Reference Voltages	$_{IN}$	0.3 VCC to 0.7 VCC		V
Output Timing Reference Voltages	$_{OUT}$	0.5 VCC		V

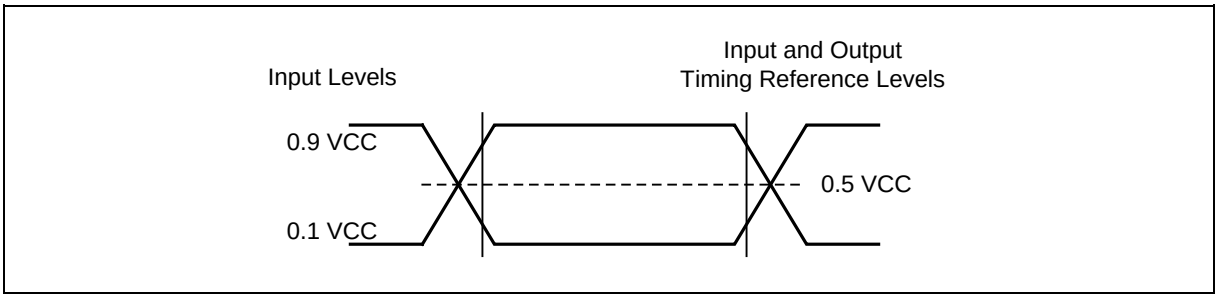


Figure 31. AC Measurement I/O Waveform

8.6 AC Electrical Characteristics(3)

DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
Clock frequency for all instructions	F_R	f_{C1}	D.C.		104	MHz
Clock High, Low Time for all instructions	t_{CLH}, t_{CLL}(1)		4			ns
Clock Rise Time peak to peak	t_{CLCH}(2)		0.1			V/ns
Clock Fall Time peak to peak	t_{CHCL}(2)		0.1			V/ns
/CS Active Setup Time relative to CLK	t_{SLCH}	t_{CSS}	5			ns
/CS Not Active Hold Time relative to CLK	t_{CHSL}		5			ns
Data In Setup Time	t_{DVCH}	t_{DSU}	2			ns
Data In Hold Time	t_{CHDX}	t_{DH}	3			ns
/CS Active Hold Time relative to CLK	t_{CHSH}		3			ns
/CS Not Active Setup Time relative to CLK	t_{SHCH}		3			ns
/CS Deselect Time (for Array Read → Array Read)	t_{SHSL1}	t_{CSH}	10			ns
/CS Deselect Time (for Erase, Program or Read Status Registers → Read Status Registers)	t_{SHSL2}	t_{CSH}	50			ns
Output Disable Time	t_{SHQZ}(2)	t_{DIS}			7	ns
Clock Low to Output Valid	t_{CLQV}	t_V			7	ns
Output Hold Time	t_{CLQX}	t_{HO}	2			ns
/HOLD Active Setup Time relative to CLK	t_{HLCH}		5			ns
/HOLD Active Hold Time relative to CLK	t_{CHHH}		5			ns

Continued – next page

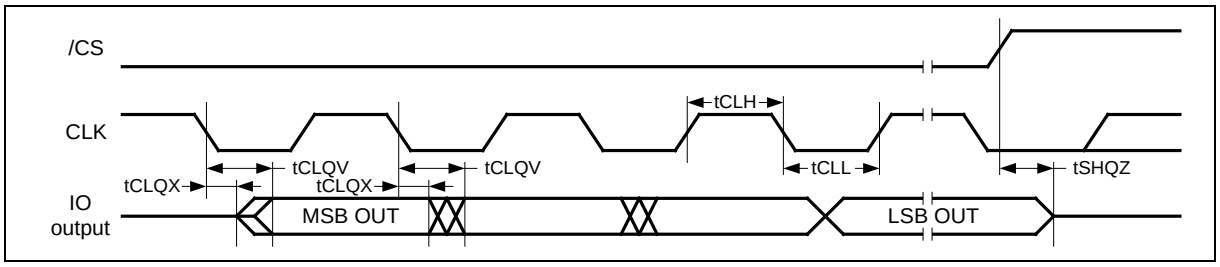
AC Electrical Characteristics (cont'd)

DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
/HOLD Not Active Setup Time relative to CLK	t_{HHCH}		5			ns
/HOLD Not Active Hold Time relative to CLK	t_{CHHL}		5			ns
/HOLD to Output Low-Z	t_{HHQX}(2)	t_{LZ}			7	ns
/HOLD to Output High-Z	t_{HLQZ}(2)	t_{HZ}			12	ns
Write Protect Setup Time Before /CS Low	t_{WHSL}		20			ns
Write Protect Hold Time After /CS High	t_{SHWL}		100			ns
Status Register Write Time	t_W				50	ns
/CS High to next Instruction after Reset during Page Data Read / Program Execute / Block Erase	t_{RST}(2)				5/10/500	µs
Read Page Data Time (ECC disabled)	t_{RD1}				25	µs
Read Page Data Time (ECC enabled)	t_{RD2}				60	µs
Page Program, OTP Lock, BBM Management Time	t_{PP}			250	700	us
Block Erase Time	t_{BE}			2	10	ms
Number of partial page programs	NoP				4	times

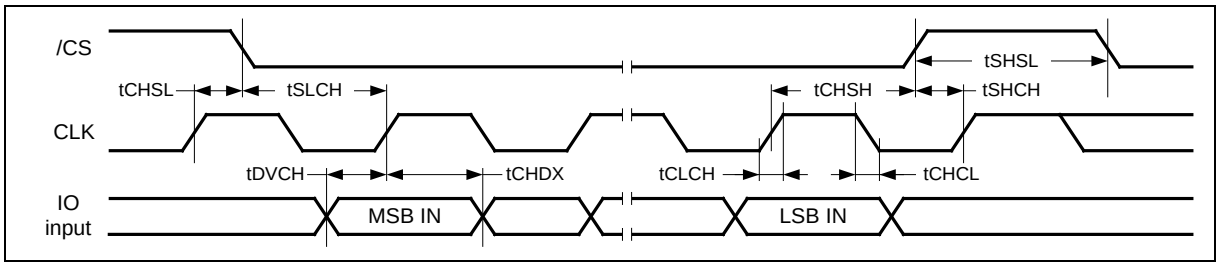
Notes:

1. Clock high + Clock low must be less than or equal to 1/f_C.
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Tested on sample basis and specified through design and characterization data. TA = 25° C, VCC = 3.0V.

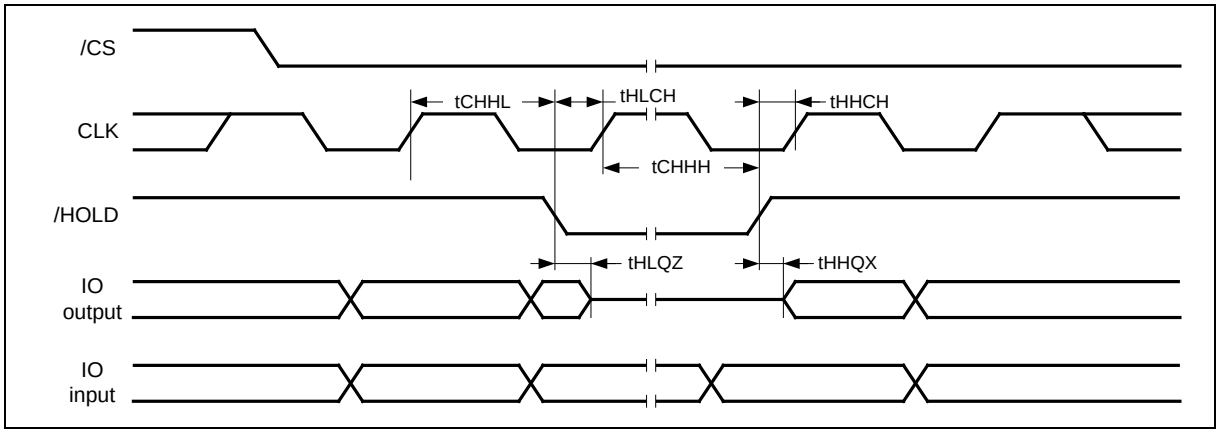
8.7 Serial Output Timing



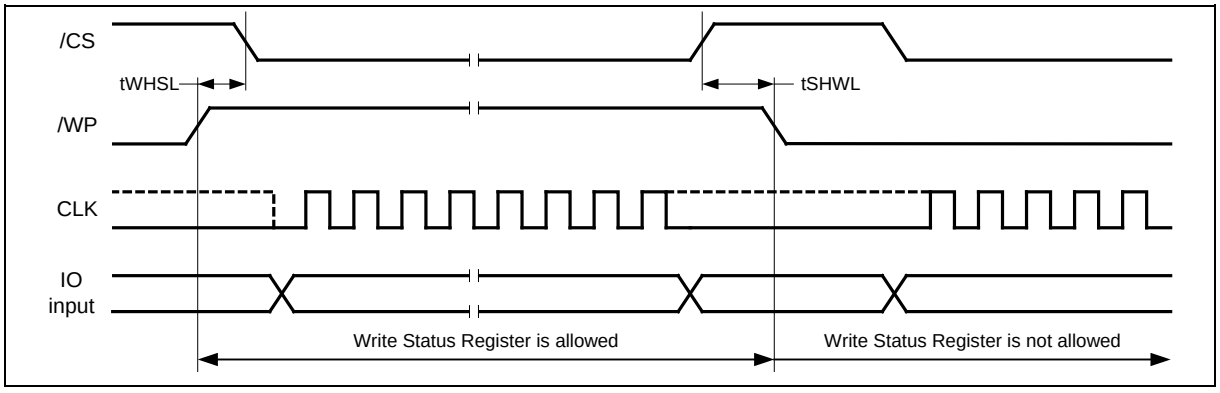
8.8 Serial Input Timing



8.9 /HOLD Timing



8.10 /WP Timing



9. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A	06/13/2013		New Create Preliminary
B	11/26/2013		Overall updates
C	12/13/2014	63, 65, 66 11 17, 26	Removed SOIC-16 package, updated order information Updated Figure.3 for device operation Changed BUF bit default value to 1 after power up
D	03/23/2015	6, 10-11, 25, 63-64	Updated W25N01GVxxIG/IT part number definitions
E	06/08/2015	25 58 60	Updated FFh Reset command description Updated tRD2 in AC parameter table Updated WSON 8x6mm dimensions
F	07/08/2015	34 All	Updated instruction description Removed Preliminary designator
G	03/21/2016	8, 62, 65, 66	Added SOIC-16 package, updated order information
H//I	08/20/2017	N/A 6, 32, 40, 41, 44-47 18 22 27 48	Modified for MCP W25M121AV *SPISTACK* Datasheet Updated Hold Pin description and Quad Mode Updated W25N01GV SPISTACK Device ID Updated Device Reset Table. Updated BBM instruction description. Updated OTP Lock Lock Description

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